2

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TESTABILITY DESIGN RATING SYSTEM: Testability Handbook

Raytheon Company

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13. ABSTRACT (Maximum 200 words)

This effort provides a means of rating the testability of an electronic design at any stage in the design life.

Volume I, Testability Handbook, discusses the particulars of the circuit design and how they relate to testability. It also discusses the software developed in this program and how to obtain the software. The software, which will run on any IBM compatible PC having 512 k of available memory and a hard disk, asks a number of questions, and based on the answers, will provide a testability rating and a credibility rating.

Volume II provides means of doing the testability analysis without the computer.

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EXECUTIVE SUMMARY

The purpose of the Testability Design Ratinḡ System (TDRS) contract was to develop a method of rating a de·ign's inherent testability and provide recommendations on how to improve the design's testability. The TDRS was developed by creating a methodology, implemented in a Personal Computer (PC) program which rates the testability of a design and a corresponding TDRS testability handbook which has recommendations on how to improve a design's testability.

The TDRS Testability Handbook is a two vc'ıme set. Volume One contains this TDRS executive summary, a TDRS introduction, and recommendations on how to improve the testability aspects of a design. Volume One, Section 1 is an introduction to Volume One and contains a description of each sectioⁿ within Volume One (pages 1-8 and 1-9). Volume One includes a list of acronyms and abbreviations before the main sections. It also includes a Bibliography and Glossary after the main sections.

Volume Two contains a copy of this executive summary and a listing of all the parameters and equations that are used in the TDRS computer program to rate a design's testability. It also contains the instructions and data needed to manually generate a testability rating.

The TDRS contract requirements were fulfilled in four phases, Each phase fulfills a major part of the TDRS development. These four phases are as follows:

PHASE ONE;

The objectives of Phase One were to determine the specific design-related parameters, associated with state-of-the-art designs, which impact testability.

Testability parameters were gathere:ᵈ by interviewing testability experts specializing in various technologies and by reviewing several hundred articles from technical proceedings, technical journals, books, and manuals. All of the resources used to gather testability data are included in the Bibliography of the TDRS: Volume I, Testability handbook.

PHASE TWO;

The objectives of Phase Two were to determine the relative impact of each parameter identified in phase one on the testability of a design.

Each parameter gathered in Phase One was assigned a testability weight based on the parameters relative overall impact on a design's testability.

PHASE THREE;

The objectives of Phase Three were to develop a rating system software package and a corresponding handbook which can measure the relative testability of a design and provide recommendations to improve the inherent testability of that design.

The rating system was developed as an executable PC program. A relational data base development tool, R:BASE, was used to generate the rating system code. The generation of the TDRS code used an R:BASE Compiler and does not require a licence from the R:BASE manufacturer. Since the TDRS program is executable, it can be run on any IBM compatible PC with DOS revision 3.1 or greater. A testability rate can also be generated manually by using the procedure and data in the TDRS testability handbook, volume two.

Recommendations on how to improve a design's testability are included in the TDRS Testability Handbook, Volume One. Each testability parameter used to generate a rate has an action associated with it. Each action refers to a section of the TDRS testability handbook which describes testability recommendations for that parameter. If a parameter is considered unresolvable, then the corresponding action is not applicable.

PHASE FOUR;

The objectives of Phase Four were to validate the TDRS by applying it to at least three (3) different Air Force designs and have an independent panel of testability experts verify the rates.

Nine MKXV designs were independently analyzed by both the TDRS program and a panel of testability experts. MKXV is an Air Force IFF (Information Friend or Foe) program. The designs consisted of three (3) MKXV Line Replaceable Units (LRUs) and six Module/Circuit Card Assemblies (CCAs) within the LRUs.

The independent MKXV analyses were performed by testability experts from Raytheon using a customized version of MIL-STD-2165. The testability experts also provided a testability rating for each design based on their own personal opinions.

The MKXV designs were then analyzed using the TDRS software. The results of the TDRS analysis was compared to the customized 2165 analysis and the expert opinions. The variance between the TDRS and customized 2165 analyses were within 17 %. The variance between the TDRS and the testability experts opinions were within 12 %.

CONTENTS

FIGURES

TABLES

PREFACE

This is the final technical report delivered by Raytheon Company to Rome Laboratory as required by the Testability Design Rating System (TDRS) contract (#30602-89-C-0121).

This is Volume One (1) of a two (2) volume set. The title of this volume is the Testability Design Rating System: Volume I, Testability Handbook. The executive summary, included in both volumes, describes the TDRS project.

ABBREVIATIONS AND ACRONYMS

A/D	Analog to Digital
ABEL	Advanced Boolean Equation Language
ADC	Analog to Digital Converter
AFC	Automatic Frequency Control
AFLC	Air Force Logistics Command
AFSCP	Air Force Systems Command Panel
AGC	Automatic Gain Control
AIDME	Army's Integrated Diagnostics in the Maintenance Environment
ALE	Address Latch Enable
ALU	Arithmetic Logic Unit
AMWC	Advanced Memory Write Control
ANSI	American National Standards Institute
AS	Advanced Schottky
ASIC	Application Specific Integrated Circuit
ASTEP	Advanced System Testability Evaluation Program
ATE	Automatic Test Equipment
ATLAS	Abbreviated Test Language for All Systems
ATPG	Automatic Test Pattern Generation
ATVG	Automatic Test Vector Generator
BEA	Built-in Test Effectiveness Analysis
BER	BIT Error Rate
FBA	False BIT Alarm
BILBO	Built-in Logic Block Observer
BIST	Built-in Self-Test
BIT	Built-in Test
BITE	Built-in Test Equipment

BIU	Bus Interface Unit
CAD	Computer-Aided Design
CAE	Computer Aided Engineering
CAFIT	Computer-Aided Fault Isolation and Testability Model
CAMELOT	Computer-Aided Measure for Logic Testability
CAS	Column Address Strobe
CASS	Consolidated Automated System Support
CATA	Computer Aided Testability Analysis
CCA	Circuit Card Assembly
CCEN	Condition Code Enable
CCD	Charged Coupled Device
CD	Compact Disk
CF	Credibility Factor
CFDS	Central Fault Display System
CISC	Complex Instruction Set Computer
CITS	Central Integrated Test System
CLK	Clock
CM	Configuration Management
CMOS	Complementary Metal Oxide Semiconductor
CND	Cannot Duplicate
COB	Chip-on-Board
COMET	Controllability and Observability Measure for Logic Testability
COP	Controllability/Observability Program
COPTR	Controllability-Observability-Predictability-Testability Report
CP	Clock Pulse
CPU	Central Processor Unit
CRT	Cathode Ray Tube
CTC	Clock Timer Circuit
CUT	Circuit Under Test
CW	Continuous Wave
D/A	Digital to Analog

DAC	Digital to Analog
DARPA	Defense Advanced Research Projects Agency
dB	Decibel
dBm	Decibel milliwatt
DBE	Data Bus Enable
DDS	Direct Digital Synthesizer
DFT	Design for Testability
DIN	Deutsche Industrie Nummer
DIP	Dual In-line Package
DoD	Department of Defense
DPSR	Data Processing System Requirement
DSP	Digital Signal Processor
DTA	Daisy Testability Analyzer
DUT	Device Under Test
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EDA	Electronic Design Automation
EEPROM	Electronically Erasable Programmable Read Only Memory
EIA	Electronics Industry Association
EMI	Electromagnetic Interference
EOTF	Electro-Optic Test Facility
EPROM	Erasable-Programmable Read Only Memory
ESD	Electrostatic discharge
ESDS	Extended Serial Digital Signal
ESS	Environmental Stress Screening
ETM-Bus	Element Test and Maintenance Bus
EU	Execution Unit
FACT	Fairchild Advanced CMOS TTL
FAR	False Alarm Rate
FAST	Fairchild Advanced Schottky TTL
FBD	Functional Block Diagram

FET	Field Effect Transistor
FFT	Fast Fourier Transform
FMEA	Failure Modes and Effects Analysis
FMECA	Failure Modes, Effects, and Criticality Analysis
FO	Fiber-Optic
FPLA	Field Programmable Logic Array
GaAs	Gallium Arsenide
GAL	Generic Array Logic
GIMADS	Generic Integrated Maintenance Diagnostics
GND	Ground
Gs	Gravities
HAT	Heuristic Advisor for Testability
HECTOR	Heuristic Controllability and Observability Analysis
HITAP	Hi-Testability Analysis Program
HSDB	High Speed Data Bus
HVPS	High Voltage Power Supply
HWSI	Hybrid Wafer Scale Integration
Hz	Hertz
IC	Integrated Circuit
ICAAS	Integrated Control and Avionics for Air Superiority
ICT	Incircuit Test
ID	Identification
IDSS	Integrated Diagnostic Support System
IEC	Industrial Executive Committee
IEEE	Institute of Electronic and Electrical Engineering
IEN	Instruction Enable
IFTE	Intermediate Forward Test Facility
INSTD	In-situ Testability Design
I/O	Input/Output
ISO	International Standards Organization

ISTD	In-Situ Testability Design
ITFOM	Inherent Testability Figure of Merit
IT TAP	Interactive Testability Analysis Program
JEDEC	Joint Electronic Design Engineering Council
JTAG	Joint Test Action Group
LAN	Local Area Network
LASER	Light Amplification by Stimulated Emission of Radiation
LCC	Life Cycle Cost
LCCB	Local Configuration Change Board
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LFSR	Linear Feedback Shift Register
LOGMOD	Logic Model
LONGMOD	Longendorfer Model
LRU	Line Replaceable Unit
LSI	Large Scale Integration
LSSD	Level Sensitive Scan Design (IBM)
MATE	Modular Automatic Test Equipment
MER	Message Error Rate
MIC	Microwave Integrated Circuit
MILMOD	Military Model
MIL-STD	Military Standard
MIMIC	Microwave/Millimeter-Wave Monolithic Integrated Circuit
MIPS	Microprocessor Without Interlocking Pipeline Stages
MIPS	Million Instructions per Second
MISR	Multiple Input Shift Register
MMIC	Monolithic Microwave and Millimeter Wave Integrated Circuit
MOS	Metal Oxide Semiconductor
MoST	Modular Scan Technique
MSDS	Minimum Serial Digital Signal

MTBF	Mean Time Between Failures
MTTR	Mean Time to Repair
MUX	Multiplexer
MWIS	Minimum Working Instruction Set
NEOF	No Evidence of Failure
OCMS	On Chip Maintenance System
OML	Organizational Maintenance Level
OMS	On-board Maintenance System
OSHA	Occupational Safety and Health Administration
PAL	Programmable Array Logic
PC	Personal Computer
PCB	Printed Circuit Board
PGA	Pin Grid Array
PLA	Programmable Logic Array
PLD	Programmable Logic Device
PN	Pseudo-Random Number
PREDICT	Probabilistic Estimation of Digital Circuit Testability
PROM	Programmable Read Only Memory
PROTEST	Probabilistic Testability Analysis
PS	Power Supply
PSCB	Programmable Silicon Circuit Board
PWB	Printed Wiring Board
RADC	Rome Air Development Center
RAM	Random Access Memory
RAS	Row Address Strobe
RC	Resistance and Capacitance
RISC	Reduced Instruction Set Computer
RF	Radio Frequency
RFI	Radio Frequency Interference

RL	Rome Laboratory
RLC	Resistance, Inductance, and Capacitance
RMS	Root Mean Square
ROM	Read Only Memory
RSS	Root Sum of Squares
RTDS	Real Time Digital Signal
S&A	Safety and Arming
SBM	Scan Bus Master (P1149) - Texas Instruments
SCOAP	SANDIA Controllability/Observability Program
SITS	System Integrated Test System
SMT	Surface Mount Technology
SQA	Software Quality Assurance
SRAM	Static Random Access Memory
SRL	Shift Register Latch
SRU	Shop Replaceable Unit
SSI	Small Scale Integration
STAGAN	Statistical Fault Analysis
STAMP	System Testability and Maintenance Program
STD	Standard
TAB	Tape Automated Bonding (COB)
TAP	Test Access Port (IEEE 1149.1)
TDES	Testability Design Expert System
TDI	Test Data In (IEEE-STD-1149.1)
TDO	Test Data Out (IEEE-STD-1149.1)
TDRS	Testability Design Rating System
TEA	Test Engineers Assistant
TFOM	Testability Figure of Merit
TFN	Thin Film Network
TITUS	Testability Implementation and Test-Generation Using Scan; AT&T
TM Bus	Test and Maintenance Bus
TMEAS	Test Measurement Program

TMR	Triple Modular Redundancy
TMS	Test Mode Select (IEEE-STD-1149.1)
TPS	Test Program Set
TRD	Test Requirements Document
TRS	Test Requirements Specification
TTL	Transistor Transistor Logic
USAF	United States Air Force
UUT	Unit Under Test
VHDL	VHSIC Hardware Descriptive Language
VHSIC	Very High Speed Integrated Circuit
VICTOR	VLSI Identifier of Controllability, Testability, Observability, and Redundancy
VLSI	Very Large Scale Integration
VSWR	Voltage Standing Wave Ratio
WSI	Wafer Scale Integration
WSTA	Weapon System Testability Analyzer

SECTION 1. INTRODUCTION

1.0 OVERVIEW.

The Testability Design Rating System (TDRS) was developed by Raytheon Company for Rome Laboratory (Rome Lab) under contract F30602-89-C-0121.

The Testability Design Rating System (TDRS) is a software program, augmented by a testability handbook, which can be used by an engineer to characterize the attributes and qualities of a ground or avionic design that make it easy or difficult to test. The TDRS is applicable to Printed Circuit Boards (PCBs) and systems/subsystems containing PCBs. It can be applied in the early stages of the design cycle to various configuration levels of hardware, including PCBs, Shop Replaceable Units (SRUs), Line Replaceable Units (LRUs), Subsystems, and Systems to analyze the inherent testability of the design. The TDRS is also capable of recommending design changes to enhance testability.

During the development of the TDRS, testability data was gathered through consultations with testability experts of various technologies, and from books, journals, and various conference papers (see the Bibliography). The definition of testability as defined and used in the TDRS program is as follows:

> "Testability is an aspect of a design which influences ease of development and thoroughness of tests, limits cost and time incurred by test development, test, and test support".

1.1 TDRS Development.

In application, the TDRS program applies several algorithms to the results of a user question and answer session. Each set of questions is used to determine the impact of specific design-related parameters which affect the design's overall testability.

The testability parameters were gathered by interviewing testability experts specializing in various technologies and by reviewing several hundred articles from technical proceedings, technical journals, books, and manuals. All of the resources used to gather testability data are included in the Bibliography of the TDRS: Volume I, Testability Handbook.

The parameters were listed and weighted based on the level of impact that they have on testability. The parameter weights were gathered during interviews with testability experts or inferred from testability literature. The parameter weights were normalized and parameters which could have a critical effect on testability were given a second more sensitive weight.

Questions were generated for each testability parameter for use in the TDRS user interactive question and answer session. Parameter algorithms were generated for each which use the user responses to rate the testability impact of each parameter for the design being analyzed.

The testability parameters were grouped into subjects. Subject algorithms (that use the parameter algorithm results) were developed to generate subject ratings from 0 to 100.

Two methods of averaging the subject ratings were created. The first method uses weights for each subject based on the relative testability impact of the subject technology compared to the other subject technologies, i.e. each subject weight is multiplied by the number of components that exist in each subject for the design under analysis. The second method generates subject weights by summing the results of multiplying each component by it's MIL Handbook 217E failure rate.

All of the algorithms mentioned above are described in mcre detail in Volume II.

1.2 TDRS Verification.

The TDRS results were verified by analyzing 9 MKXV designs using the TDRS software and comparing the results to an independent testability rating technique and the subjective opinions of testability experts.

MKXV is an Air Force IFF (Identification Friend or Foe) program. The designs analyzed consisted of three (3) MKXV Line Replaceable Units (LRUs) and six Module/Circuit Card Assemblies (CCAs) within the LRUs. These designs were chosen because they represent a broad spectrum of technologies. By choosing MKXV designs for this activity, a "real" rather than "simulated" analysis was accomplished since these items were actually new Raytheon designs.

The method used by the experts to analyze each design was a generic procedure which was developed by the testability experts. It used a customized version of MIL-STD-2165. The results of these analyses were testability rate assessments between 0 and 100. The testability experts also provided their own subjective rate assessment of the design's testability between 0 and 100 based on their experience and expertise.

The MKXV designs were also analyzed using the software and associated handbook which comprises the "Testability Design Rating System". The TDRS generated a rate for every testability subject which was applicable to each design and a final rate. The TDRS testability subjects consist of 16 groups of independent testability parameters sorted mainly by technology.

All of the designs were analyzed using the TDRS software. One of the designs was also analyzed using the manual analysis procedure contained in Volume II of the TDRS handbook. The results of this manual analysis agreed with the software analysis.

The results of the TDRS analysis were compared to the customized 2165 analysis and the experts opinions. The variance between the final rate of the TDRS and customized 2165 analyses was within ±17 %. The variance between the final rate of the TDRS and the testability experts opinions was within ±12 %.

A summary of the analyses mentioned above and the variance between them is listed in Table 1.

Table 1-1. TDRS Verification Results

Type of Assembly	Customized MIL-STD-2165	Independent Analyst's Opinion	TDRS Testability Rate/CF	TDRS % Variance 2165/Opinion
LRU	88	88	84/41	-4.5/-4.5
SRU	85	85	75/69	-11.8/-11.8
SRU	84	75	71/70	-15.5/-5.3
SRU	69	80	80/80	13.8/0
LRU	88	88	91/42	3.3/3.3
SRU	86	90	86/69	0/-4.4
SRU	82	90	98/93	16.3/8.2
LRU	88	88	91/42	3.3/3.3
SRU	76	90	89/94	14.6/-1.1

1.3 TDRS Software.

The TDRS is designed to present a comprehensive understanding of the testability of a design. It provides easy access to information about a particular testability parameter as well as recommendations on solutions to related testability problems. It also permits acquiring information pertinent to a testability rating. The rating scheme provides a final testability rating and credibility fac.or with detailed sub-ratings and sub-credibility factors used to generate the final rating.

The output of the TDRS program includes the testability rating, rating credibility factor, testability parameters, concerns, and actions which are described below:

> The Testability Rating (TR) is simply a number, ranging from 100 down to 0, indicating the degree of testability of a design which was analyzed. The relevance of the TR ranges from "excellent testability" (100) (no concerns nor actions) to "completely untestable" (0). The TR is generated based on a user s responses to questions about testability parameters. After a TR is generated it is stored in the TDRS data base.
>
> The rating Credibility Factor (CF) is a number supplemental to the TR which describes how credible the TDRS testability rate is. It ranges from 100 down to 0. A higher number corresponds to a more reliable analysis. It is generated by the TDRS software based on the number and importance of testability parameter questions that the user could answer versus those that the user "could-not-answer". A testability parameter question that the user "could-not-answer" may be due to lack of information, documentation, or time to answer it. After a CF is generated it is stored in the TDRS data base with the corresponding testability rating.
>
> A testability parameter is a unique aspect of a design which has an impact on the testability of the design. Independent sets of testability parameters are grouped into testability subjects.
>
> A testability concern exists for each parameter and briefly describes why that parameter is important for testability.
>
> A testability action exists for each parameter and concern. A concern may or may not be resolvable. An unresolvable concern would be an instance where, due to uncontrolable factors (technological, physical, etc.), the problem cannot be improved with design changes. If a concern is unresolvable, then the corresponding action is Not Applicable (N/A). If it is resolvable, then the action will be a reference to a section of the TDRS testability handbook for recommendations on how to resolve the concern.

The TDRS program is a menu driven software package. It is an executable program developed using R:BASE, a relational data base development tool. The software flow depends on user menu selections during the program execution. Additionally, a HELP screen can be accessed from each menu in the program.

A more detailed description of the TDRS software can be found in the second volume of this handbook - Testability Design Rating System: Volume Two - Analysis Procedure.

In summary, the TDRS computer-based, menu-driven, software package, augmented by a testability handbook, rates the testability of an electronic design and presents a testability rating, rating credibility factor, testability parameters, concerns, and actions. It can also report a history of part numbers, ratings, a hierarchical tree of part numbers, and rating credibility factors for any part number previously analyzec.

For a descriptio.i of how to use the TDRS , consult the TDRS TUTORIAL located in the TDRS software program.

For a description of how a testability rating and credibility factor are generated, consult the TDRS SCORING AID located in the TDRS software.

1.4 TDRS Software Requirements.

The following is a list of the requirements needed to run the TDRS software:

1. An IBM PC or compatible computer,
2. DOS version 3.1 or higher,
3. 512 Kbytes of available memory,
4. 2 Megabytes of hard disk memory,
5. A 5 1/4 inch floppy disk drive.

1.5 TDRS Software Installation.

The TDRS software can be installed on any computer which meets the requirements stated in paragraph 1.4. Prior to loading the TDRS software, the C:\CONFIG.SYS files must exist with the following lines:

```
FILES   = 20        (20 or higher)
BUFFERS = 25        (25 or higher)
```

The TDRS software can be installed on either a 360 K or 1.2 Meg floppy disk drive. The TDRS software exists on three 360 K floppy disks which can be loaded with either drive.

To install the TDRS program, insert the floppy disk labeled "TDRS 360 K disk 1" into the disk drive. At the keyboard, type; X:INSTALL X Y (where X is the drive where the floppy disks are being loaded from and Y is the target drive to load the software to).then press [ENTER]. Typically, the TDRS software is loaded from the A: drive to the C: hard disk drive and the installation command would be - A:INSTALL A C. The computer will automatically prompt the user to install the remaining two disks in the floppy disk drive.

To initiate the TDRS program, type; CD Y:/TDRS, then press [ENTER] (where Y is the drive which the software was loaded to). Then, type; TDRS, and press [ENTER] again.

1.6 Handbook Overview

The complexity and density of today's electronic assemblies have made testing and fault isolation major cost factors in the design verification, manufacturing, and support phases of a product's life.Testing and fault isolation are often more expensive than material and construction cost. Engineers today must design circuits that can be tested in an efficient and orderly way. Incorporating ease of testing in the design facilitates fault isolation and helps lower maintenance costs over the life span of the product.

This handbook has three objectives: (1) to define testability, (2) to make the designer aware of testability, and (3) to give a clear understanding of how the designer can implement testability into designs. The information contained herein establishes guidelines which represent the collected experiences from many programs and the personal experiences of many engineers, technicians, and manufacturing personnel.

This handbook cannot cover all conditions and situations, but it does describe the fundamental issues and test-related design problems most commonly encountered. The intent is to provide the designers with ideas and approaches so that the design program end result is a product that can be tested and maintained at minimum cost.

The benefits of designing for testability can be realized by the individual and the entire organization. Some of the benefits of designing for testability are as follows:

- Reduction of the time required to transfer a design from Design Engineering to Manufacturing Engineering.
- Reduction of post release involvement on the part of the Design Engineer to get a design smoothly incorporated into the production line.
- Reduction of the cost of manufacturing and as a result increase profits.
- Introduction of products with a lower initial and life cycle cost, which will serve to increase product sales and increase market share.
- Decreased test times and improved delivery schedules.
- Increased Field Service productivity by allowing more efficient diagnosis and repair.

1.6.1 Testability Awareness. Testability is not a technological innovation. It is a way of thinking wherein the designer possesses an awareness of the importance of testing. Testability is designed in at the beginning of the design process. The proper time is when the system, PCB, etc., is being initially designed. Any other time cannot prove to be as cost effective.

Because testing is an unavoidable function, and every bit as critical as gain, bandwidth, or impedance matching, the designer must think of testability as part of the specification that the design must meet. Before starting any design, the designer should ask himself, "How will I test it, how will production test it, and how will it be tested in the field?" It is the designer's responsibility to have these answers prior to beginning a design, and to ensure that only testable designs are released to production.

Frequent, lengthy unplanned test and fault isolation activities result in significant cost and schedule overruns as well as an accompanying loss of product credibility. In some instances, especially where large scale integration (LSI) and very large scale integration (VLSI) devices are utilized, unless the engineer has designed the hardware/software from the start to facilitate testing, fault isolation, and maintenance, the task of adding testability is likely to be impractical. Other factors to consider are the time required to effect the transfer from engineering to the manufacturing facility, and the required post- release involvement of the design engineer. These factors all contribute to a decrease in manufacturers competitiveness.

The selection process for test equipment and test software must also be initiated at the start of the program. The selection of these potentially expensive and critical items, which will be used at the various stages of the product's life cycle, is as important as the product's inherent testability. Equipment and software that is in place or planned for the engineering and/or manufacturing facility or the customer's inventory must be evaluated against equipment which is new or conveniently available. Standardization among the various testing sites is the objective; thus close communication between Program Management, Engineering, Manufacturing, and the Customer must be ongoing to ensure cost-effective utilization of these valuable resources.

Testability does not just happen, it requires a conscious effort on the part of the designers during the initial design of a product. It is the designer's responsibility to ensure that only testable designs are released to production. Each designer must make a commitment to designing products that are testable in design, manufacture, and service.

1.6.2 Implementation. To aid designers in meeting the testability objectives, this Handbook may be used as a guide in avoiding recognized problem areas. The inherent testability of a design can be evaluated using the Testability Design Rating System at critical points in the design process.

A design review should occur prior to any release of the electrical schematic or logic diagram to artwork/layout and also at the transition to production phase. The results of these evaluations, and any corrective action should be approved by a testability engineer assigned to the particular program. The results should also be used as a design review input.

A Testability Program Plan should be written for each program, based on tailored requirements from MIL-STD-2165, including among other considerations, the following:

- Testability objectives (contract requirements),
- Test subsystem concept,
- Test facilities (Development, Manufacturing, Field),
- Documentation requirements,
- Organizational responsibilities (Laboratory, Manufacturing, Program Management),
- Guidelines and standards.

1.7 Handbook Structure.

The information contained in this handbook has been separated into the following major sections:

- Abbreviations and Acronyms - A list of commonly used testability acronyms and abbreviations.

- Generic Testability,(top level) (Section 2) - Presents testability recommendations which are generic and applicable to any type of design and configuration.

- System/Subsystem (Section 3) - Presents an overview of the testability tasks performed at the system level from the concept phase to any subsequent phase. It contains a description of the definition and development of system requirements and specifications, planning of the testability effort, and universal suggestions for enhancing the testability of system hardware.

- System BIT (Section 4) - Describes various aspects of Built-in-Test (BIT) and provides recommendations on how to implement BIT at system level.

- Module (Section 5) - Presents testability recommendations which are applicable to all designs at the module level of configuration.

- Module BIT(Section 6) - Describes built-in-test (BIT) at the module level and provides implementation recommendations.

- General Digital (Section 7) - Presents the concepts of initialization, visibility, and partitioning for digital designs. Also includes some general and specific guidelines for SSI/MSI digital designs.

- LSI/VLSI (Section 8) - Expands on the concepts presented in section 3 and how LSI/VLSI designs can be improved for testability.

- Microprocessors/Support Chips (Section 9) - Describes testability suggestions and provides testability recommendations for all types of presently available processors and support chips.

- Memory Devices (Section 10) - Presents testability recommendations for memory devices.

- Structured Design-for-Test (DFT) Techniques - Scan/Boundary Scan (Section 11) - Presents the concept of structured design-for-test including boundary scan and its implementation as IEEE Standard 1149.1.

- Analog (Section 12) - Describes methods for improving observability and controllability of analog circuits through test point selection and partitioning. Specification guidelines and ATE interfacing are also discussed.

- High Frequency (Section 13) - Covers such topics as partitioning, test points, and test equipment limitations for high frequency designs. Specific guidelines for RF, Microwave, and Monolithic Microwave Integrated Circuits (MMIC) are also included in this section.

- High Power (Section 14) - Provides testability and safety recommendations for all high power devices.

- Incircuit (Section 15) - Analyzes in-circuit test techniques and details testability guidelines necessary when using these techniques.

- Electro-Optics (Section 16) - Describes electro-optics testability.techniques

- Others (Electro-Mechanical and Other Technologies: Section 17) - Provides testability recommendations for electro-mechanical and other topics not covered above.

- Bibliography - List all references used in developing this report.

- Glossary - A list of commonly used testability terms used in this handbook and elsewhere.

1.8 OBTAINING THE SOFTWARE

The software from this program may be obtained from the Defense Technical Information Center (DTIC), Cameron Station, Alexandria VA 22304-6145 or by phone (703)274-7633, or DSN 284-7633. Release of this software by DTIC requires that both Government agencies and Government contractors send a completed set of Terms and Conditions (see next page) to RL/ERSR, Griffiss AFB NY 13441-5700. In addition, contractors must send a copy of their approved DD Form 2345.. Information on the DD Form 2345 may be obtained from the United States/Canada Joint Certification Office, 74 N. Washington, Battle Creek MI, USA 49017-3084 or by telephone at 1-800-352-3572.

If you have any questions, call the Project Engineer Roy F. Stratton at (315)330-4205.

Requests to DTIC should reference the AD number:
AD-M200 073L

STATEMENT OF TERMS AND CONDITIONS RELEASE OF AIR FORCE OWNED OR DEVELOPED COMPTUER SOFTWARE PACKAGES

Date ______________

1. Release of the following US Air Force software package (computer programs, systems descriptions, and documentation) is requested:

Rome Laboratory's Testability Design Rating System

2. The requested software package will be used for the following purpose:

Such use is projected to accrue benefit to the Government as follows:

3. I/We will be responsible for assuring that the software package received will not be used for any purpose other than shown in Paragraph 2 above; also, it will not be released to anyone without prior approval of the Air Force. Further, the release of the requested software package will not result in competition with other software packages offered by commercial firms.

4. I/We guarantee that the provided software package, or any modified version thereof, will not be published for profit or in any manner offered for sale to the Government; it will not be sold or given to any other activity or firm, without the prior written approval of the Air Force. If this software is modified or enhanced using Government funds, the Government owns the results, whether the software is the basis of, or incidental to a contract. The Government may not pay a second time for this software or the enhanced or modified version thereof. The package may be used in contract with the Government but no charge may be made for its use.

5. The US Air Force is neither liable nor responsible for maintenance, updating or correcting any errors in the software provided.

6. I/We understand that no material subject to national defense security classification or proprietary rights was intended to be released to us. I/We will report promptly the discovery of any material with such restrictions to the Air Force approving authority. I/We will follow all instructions concerning the use or return of such material in accordance with regulations applying to classified material, and will make no further study, use, or copy such material subject to security or proprietary rights marking.

7. I/We understand that the software package received is intended for domestic use only. It will not be made available to foreign Governments nor used in any contract with a foreign Government

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SECTION 2. GENERAL TESTABILITY GUIDELINES (Top Level)

2.0 OVERVIEW.

Generic testability refers to all parameters that affect the testability of any type of design independent of the technology or level of configuration of the design. Generic testability correlates to the subject "Top Level" in the TDRS software.

2.1 Documentation.

The following paragraphs deal with the design and scope of the documentation supporting a module, LRU, unit, subsystem, or system. Although it may seem only a secondary consideration to many, well-designed documentation can greatly improve the testability of a particular UUT or program.

2.1.1 Hardware Documentation. The purpose of hardware documentation is to provide both factory and field test personnel with all the material relevant to the operation and troubleshooting of the hardware assembly. The information must be structured to make troubleshooting as easy as possible. The following are items of hardware documentation.

1. Schematic diagram
2. Relevant waveforms/timing diagrams
3. Wiring diagrams and wiring run lists
4. Assembly drawings and parts lists
5. Copies of manufacturer's specification sheets for all components contained on the UUT
6. UUT functional description and theory of operation
7. Voltage/resistance chart for UUT nodes
8. List of test equipment required
9. Equipment performance specifications and test procedures
10. Test Flow
    - Block diagram
    - Brief description of tradeoffs (reasons for decisions)
    - Faults found at each test !evel (include method of measurement)
11. Interface
    - Graphic description of interface
    - Schematic
    - Wiring diagram
    - Nodal cross-reference (bed of nails)
    - Assembly diagram (include assembly drawing, bill of materials, assembly Instructions, etc. in this section)

Each documentation package should be as complete as possible, though not all UUTs will require the same level of documentation. The complexity of the UUT and the design and type of tester used will affect the documentation required. For example, a digital CCA tested on the Fluke 3010 logic tester will require a nodal counts table for all CCA nodes and a good block diagram and theory of operation. An analog CCA, tested manually, will require waveforms for appropriate nodes and a more detailed (component level) theory of operation. Each type of hardware documentation is described in detail below.

2.1.1.1 Schematic Diagram. There are several points to keep in mind in the design and layout of the schematic diagram, which can greatly improve the testability of the UUT. These are:

- All input pins should be shown on the left of the schematic diagram, and output pins on the right. I/O pins should not be shown in the middle.

- If possible, a truth table for each digital IC (other than simple gates) should be shown on the schematic diagram. If the truth tables must be shown elsewhere, reference that document on the schematic.

- If possible, nodal counts, relevant waveforms, and/or timing diagrams should be included on the schematic diagram at the appropriate nodes. If not, the schematic should reference the document(s) containing this information. The documentation originator should number the nodes on the schematic and reference the node number on the document containing the waveforms, etc. (See figure 2-1.)

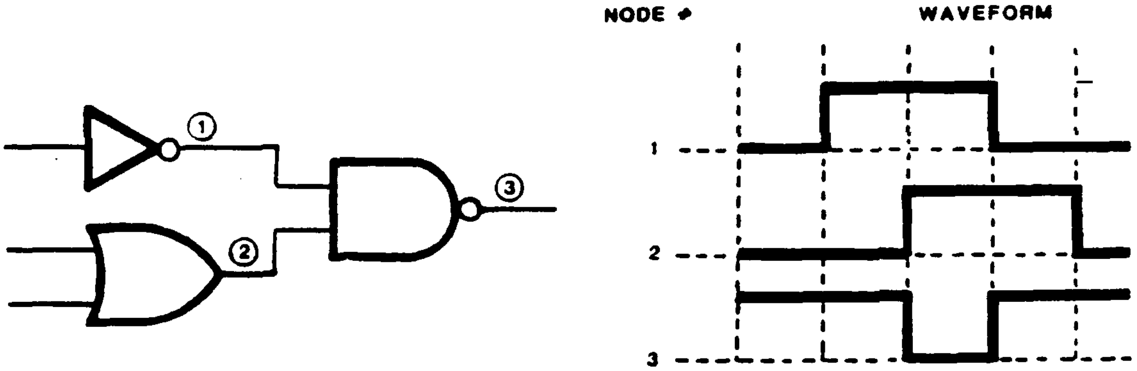


Figure 2-1. Example of Schematic Node Waveform Description

- Functional designations (CK, R/W, Q, BUSRQ, etc.) should be shown next to eacʰ IC pin number on the schematic, except on logic gates. Logic gates should have the input signal names listed at the inputs and the signal name logically formed at the output.

- Power supply circuits on non power supply CCAs should be shown in a single location on the schematic diagram and all voltages should be labeled.

- Schematic diagrams of all sub-circuits, such as vendor-supplied modules mounted on the CCA, should be provided - either on the overall schematic diagram, or supplied separately and referenced on the overall schematic diagram.

- The schematic diagram should reference the assembly drawing and give the part number of the next higher assembly.

- If the schematic diagram for a single CCA or assembly takes up more than one page, all inter-page signals should be referenced with signal name and/or number and should show zone designation and page number where signal goes to and comes from.

- Do not show a single I/O pin more than once on a schematic without cross-referencing the zone designations.

- Do not use more than one logic symbol to depict a specific component or hardware part. If a vendor-supplied module includes a schematic diagram with symbols that are different, redraw the vendor's schematic or correct those different symbols. Different representations can be very confusing to a technician or maintenance person.

- Make sure that just before the drawing is released to manufacturing that the above suggestions are not "stripped out" by an over zealous draftsman!

2.1.1.2 Relevant Waveforms/Timing Diagrams. As mentioned above, these are best shown on the schematic diagram where space permits. When shown separately, they should be referenced to the schematic diagram by schematic name and/or number, and node number. The following also are important when depicting waveforms, timing diagrams and logic diagrams.

- All voltage levels should be shown.

- If timing is important, state where oscilloscope should be triggered.

- Show all necessary specifications and tolerances (such as pulse width, rise and fall time, etc.).

2.1.1.3 Wiring Diagrams and Wiring Run Lists. Point-to-point wiring diagrams for all wiring harnesses, and wiring run lists for all wirewrap boards should be provided. These should include a list of points wired together, color and size of the wire, signal name and, in the case of a wirewrap board, the level at which the wire is wrapped to a pin. A technician can more easily trace missed wires or shorts using a wiring diagram or wiring run list rather than using a schematic diagram.

2.1.1.4 Assembly Drawings and Parts List. The assembly drawing and related parts list should be as complete and simple to read as possible. Avoid overcrowding an assembly drawing with unnecessary details. Information on the parts list should include such specific information as resistor tolerances and capacitor working voltages. This is particularly helpful when parts must be substituted due to shortages, unavailability, etc.

2.1.1.5 UUT Functional Description and Theory of Operation. This document should begin with a brief description of the function of the UUT being tested. Describe what the UUT does (i.e., memory CCA, power supply, D/A converter, etc.). Also describe how the UUT fits into the overall unit or system.

The theory of operation should begin with a block diagram description of all functional sections of the UUT. For instance, if a group of ICs for: ˉ an oscillator, they can be described as such. It would also help to label these ICs as "Oscillator" or "Master Clock Circuit", or whatever, on the schematic diagram, surrounding the ICs with a dotted line if necessary for clarity. Include a separate block diagram drawing with the description (see figure 2-2).

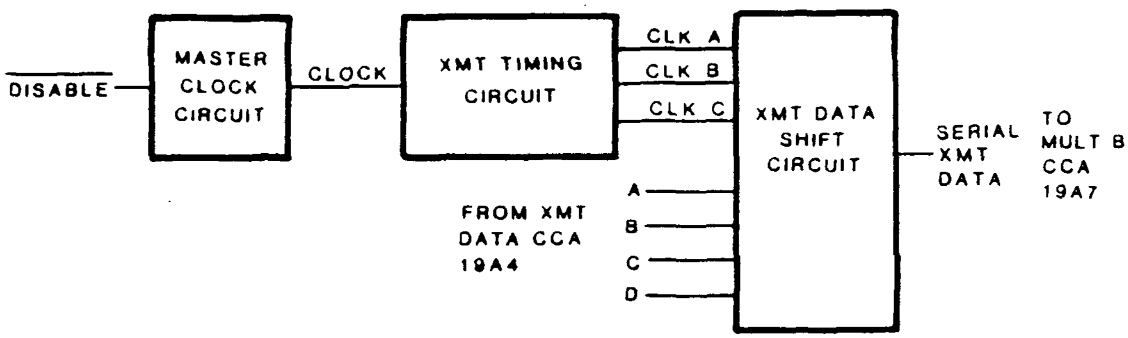


Figure 2-2. UUT Functional Block Diagram

A detailed theory of operation may or may not follow the block diagram description, depending on the detail and type of troubleshooting required, but in general, the theory of operation should always be provided. If the UUT is digital and being tested on a Fluke 3010 logic tester, a detailed theory would be nice but not necessary, since the technician will be looking for nodal counts rather than functions of specific ICs. On the other hand, if the technician is really expected to get into the circuits, node by node, with an oscilloscope, a detailed theory of operations could be vital. Remember that field maintenance personnel do not have sophisticated ATE at their immediate disposal. Also, analog circuits are always candidates for a detailed theory of operation memo. The schematic alone may not give the technician sufficient information due to the variety and complexity of most analog circuits.

2.1.1.6 Voltage/Resistance Chart for UUT Nodes. This type of chart is generally useless for digital circuits but may be helpful in analog circuits, particularly power supplies. Each node on the UUT has a resistance-to-signal (as opposed to chassis) ground when the UUT is off, and each node has a voltage level when the UUT is on. The voltage/resistance chart can supply this information to aid in troubleshooting. If this type of chart is supplied, be sure to specify the type of meter being used (i.e., a 20,000 ohms/volt multimeter, digital voltmeter,etc.).

2.1.1.7 List of Test Equipment Required. All equipment required to test the UUT should be listed and a drawing of the test setup also should be supplied. Important factors that should be noted along with the list are: part numbers of connectors required in test setup to interface with the UUT, types of coaxial cable required, and terminations or loads required in the test setup.

2.1.1.8 UUT Performance Specifications and Test Procedures. Pertormance specifications and UUT I/O tolerances should be listed. When choosing tolerances, be careful not to make them so tight that more UUTs fail than pass a test. Make a special note of unusual or abnormally tight tolerances for the technician. Test procedures should be clear and easy to follow. A step-by-step test is often the easiest type of format to follow. An alternative, especially for more complicated procedures, is a flow chart with subroutines to aid in isolating faults. No matter what type of test procedure format you choose, always provide information on what the operator or technician should do if a step and/or entire test fails.It is difficult to isolate a fault when the technician does not even know what signal or function he/she is checking in a particular step.

2.1.1.9 Typical Failure Modes. All analog and all unusual failure modes should be documented. If a failure in a circuit causes a delayed output transition, then this failure mode should be specified. Documenting such failures alerts a test program developer or technician of its possible occurrence. The test program developed may create a test to check for the failure or a technician may look for the failure during debug.

2.2 Hardware Selection.

The parts chosen for a design should be well documented or data sheets should be provided and easy to procure. Older parts which are no longer manufactured are very difficult to replace. If old discontinued parts fail then custom parts may need to be made to replace them or a partial redesign may be necessary. The same problems may result if very customized parts are used. If a similar functioning standard part exists, then it should be used rather than an obsolete or customized part (as long as it meets performance and other requirements).

2.3 Test Philosophy.

Often separate test programs are developed for production testing and depot testing. The tests are similar, however, the production test program will often undergo modifications due to operational experience. A production tester may test thousand of units Under Test (UUTs) over several years whereas a depot tester may only test twenty units during that test time period. As a result the, the production test program is often improved due to the production experience modifications. After a year of use, the production could be much more accurate than the depot tester due to modifications.

A better approach is to use the same test program developed for production test in the depot. This concept is referred to as "vertical testability". By employing "vertical testability," cost and time needed to developed test programs are reduced. Only one test program needs to be developed. When modifications are made to the production test program, a copy of the program (with a new revision number) would be sent to the depot. The depot would then have a more accurate test program with very little added cost.

Overall, using "vertical testability" saves money and time and is an efficient test philosophy.

SECTION 3. SYSTEM/SUBSYSTEM TESTABILITY GUIDELINES

3.0 OVERVIEW.

This section examines the basic objectives in designing for testability at the system/subsystem level, emphasizing the role played by the system engineer and the testability engineer in accomplishing these objectives. The major benefit of enhanced testability is lower product cost. For example, increasing the testability of a specific design to improve product yield at the manufacturing plant can lower unit production cost of the end item. Operation and support costs can in turn be lowered by improving product testability, so as to isolate faults more rapidly and without ambiguity to the field replaceable item in deployed systems.

Another benefit associated with testability is augmented system readiness. System level testability parameters are directly related to the ability of a deployed system to be operationally ready to perform required mission functions. This aspect of testability must be interrelated with all other objectives by the system planners in order to achieve a balanced design, a product whose testability characteristics meet system requirements at the lowest life cycle cost (LCC).

3.1 Testability Planning.

The basic vehicle for organizing and implementing design for testability efforts is the Testability Program Plan. The development of planning documents and the requirements necessary to define testability design specifications are also described in this section.

3.1.1 Testability Objectives. The successful completion of a design-to-test effort impacts system performance, production test, and field support. Specific goals addressed by a testability program include:

- Maximizing operational capability through the use of built-in test (BIT), which includes user friendly controls and displays. (See section 4.0)

- Optimizing equipment availability by rapid fault detection and unambiguous fault isolation.

- Reducing support system complexity by providing compatible, cost-effective test systems.

- Reducing acquisition cost by optimizing production yield through efficient testing.

- Reducing BIT/ATE test complexity by providing standardized hardware/software.

To achieve these objectives, planning must begin at the concept exploration phase and continue throughout the demonstration and validation phase. This planning process must consider:

- Diagnostic test plan
- Maintenance levels of the support system
- Factory test plan and factory test equipment (needed and/or available)
- Preventive/corrective maintenance requirements
- Throw-away versus repair decisions
- Operating environment of the system
- Support test equipment (needed and/or available)
- Environmental and/or packaging requirements
- Built-in test equipment capabilities
- Skill level of maintenance technician

3.1.2 System Testability Requirements and Specifications. The prime system testability requirements and specifications, which result from an analysis of the system utilization, the support concept, and the performance requirements must be clearly stated and allocated in a top-down process in order for the test subsystem to be effective in performance monitoring, fault detection, and fault isolation. These are fielded hardware conditions and must also be coordinated with the needs of the production facility. If done early enough in the design cycle, the proposed prime item test subsystem, whether BIT and/or ATE, and the prime item haraware itself can be configured, with very little additional hardware and/or software to ease the production test burden.

On-line BIT monitoring is the most desirable mode of operation and is dictated by the prime system and mission needs. This requires tradeoffs in cost, technical impact on the design, and the operational requirements for the mission. (See section 4.7.1).

3.1 3 Testability Program Plan Formulation. The considerations listed in paragraph 3.1.1 provide a framework for developing a set of tasks during the early phases of a program, the results of which should be documented in a Testability Program Plan. As a minimum, the following major task efforts should be accomplished during concept exploration and incorporated into the Testability Program Plan as appropriate:

- Establish the qualitative and quantitative testability requirements for the system/subsystem.

- Conduct preliminary tradeoffs to establish the test system definition and provide design criteria for system/subsystem compatibility with test philosophy.

- Incorporate testability requirements into the system/subsystem specification.

- Correlate requirements for testing the system during its assembly and checkout, and during the field support period. Unit production cost goals derived from life cycle cost data should be a major influence on the factory test approach.

Preliminary testability specifications are further developed and imposed on equipment designers during the follow-on demonstration and validation phase.

3.1.3.1 Testability Program Plan. The Testability Program Plan is a variety of information tailored to each specific program. It should contain a brief overview that will provide a functional description of the system along with its physical hardware. Testability requirements should be included; these should be extracted from the top level specification (or if unavailable they must be self-imposed) and allocated to the lowest design level appropriate for the program.

A description of the test subsystem and its compliance (or noncompliance) with the testability requirements should follow, in addition to a rationale for the test subsystem configuration. High failure rate and high risk items should be identified as well as those that are time consuming to replace. These items are also candidates for additional test points.

The test subsystem description should contain a statement of the electrical test adjustment philosophy that describes the electrical adjustments that are required during test. It should also include a discussion of (1) the features that will facilitate production testing and diagnosing to the comp:-nent level, (2) standardization between production and field testing (hardware, software, firmware), and (3) how a functioning system is recognized in both production and deployment.

Additional information needed for the plan would include a list of test equipment requirements (hardware and software) for development, production, and deployment as well as the documentation requirements (hardware, software, firmware, diagnostic and test, and a Test Requirement Specifications (TRS).

The plan should also cover such areas as (1) the assignment of responsibility for testability reviews, (2) TRS generation, (3) test and validation, (4) test grading, (5) any required demonstration planning, and (6)a testa:ility schedule of events.

3.2 Testability Requirements;.

Quantitative testability requirements are established by customer needs associated with readiness objectives. Other requirements or guidelines reflect the benefit of past experience and impact all objectives previously mentioned. The following paragraphs describe the System Engineering Process to design testability into a system/subsystem level UUT.

3.2.1 System Engineering Process. The system engineer's task is to identify the parameters, constraints, and tradeoffs imposed by the system needs/requirements. The output of this task is a consistent set of end item specifications for design. A general system testability program flow is illustrated in figure 3-1; a general testability task matrix is shown in table 3-1.

Table 3-1. Testability Task Matrix

Task	Program Phase		
	Concept	Design	Production
Testability program planning	X	√	X
Testability reviews	√	√	S
Data collection and analysis planning	X	√	√
Testability requirements	√	√	X
Preliminary testability design and analysis	X	√	S
Detail testability design and analysis	X	√	S
Testability demonstration	X	√	S

S - Selectivity applicable to design changes.

X = Not Required   √ = Required

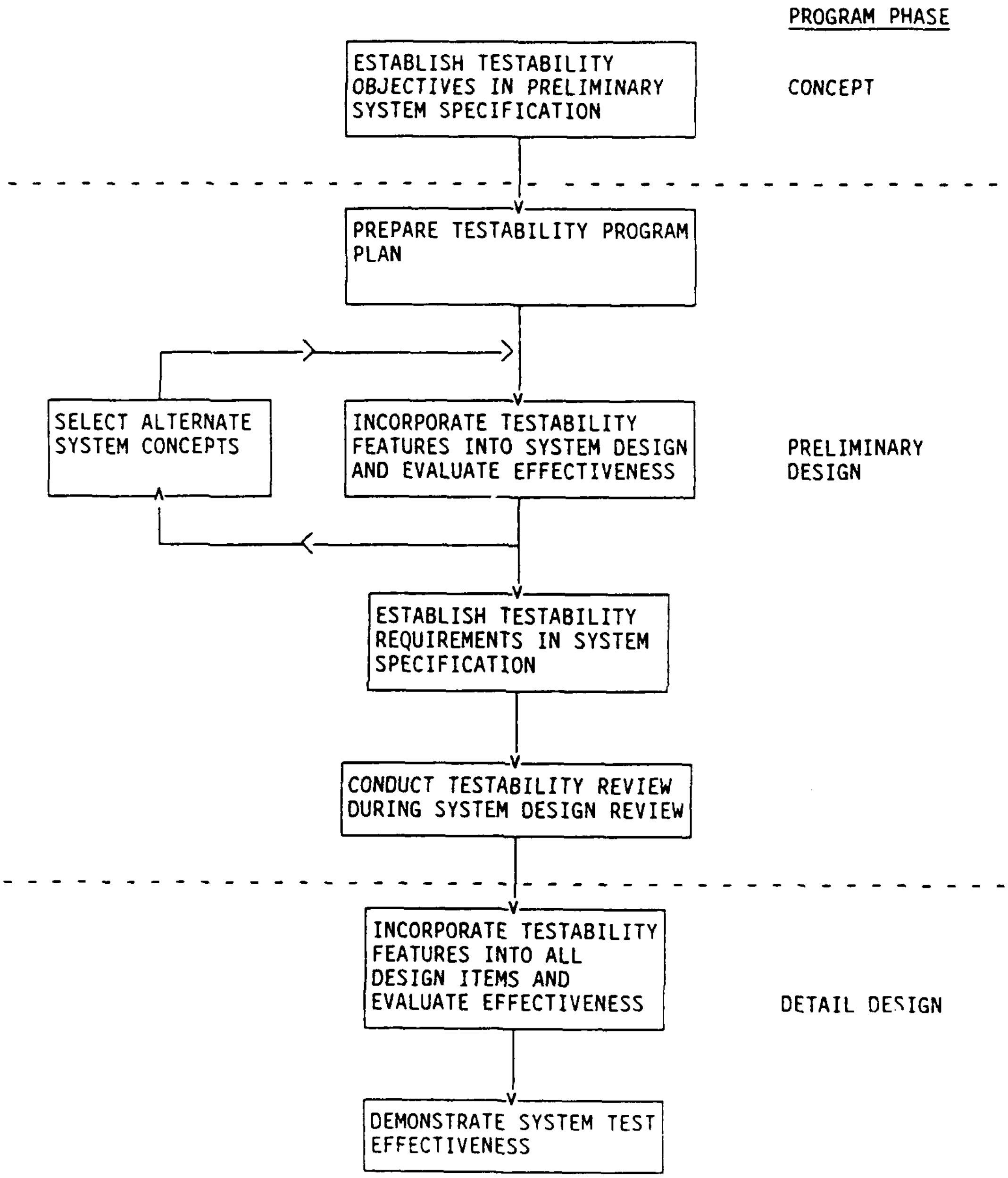

PROGRAM PHASE
ESTABLISH TESTABILITY OBJECTIVES IN PRELIMINARY SYSTEM SPECIFICATION
CONCEPT
PREPARE TESTABILITY PROGRAM PLAN
SELECT ALTERNATE SYSTEM CONCEPTS
INCORPORATE TESTABILITY FEATURES INTO SYSTEM DESIGN AND EVALUATE EFFECTIVENESS
PRELIMINARY DESIGN
ESTABLISH TESTABILITY REQUIREMENTS IN SYSTEM SPECIFICATION
CONDUCT TESTABILITY REVIEW DURING SYSTEM DESIGN REVIEW
INCORPORATE TESTABILITY FEATURES INTO ALL DESIGN ITEMS AND EVALUATE EFFECTIVENESS
DETAIL DESIGN
DEMONSTRATE SYSTEM TEST EFFECTIVENESS

Figure 3-1. System Testability Program

Basic studies must be performed by the engineering disciplines as shown in table 3-2. These tasks are coordinated, integrated, and refined to establish a set of specifications for design. Some of the factors that must be included during the tradeoffs are expanded upon in the paragraphs that follow.

Table 3-2. Testability Interfaces with Engineering Disciplines

Discipline	**Testability Related Tasks**
System Design & Test	1. Allocate readiness and performance requirements to design parameters. 2. Allocate test functions to hardware/software implementation. 3. Determine cost of alternative test approaches. 4. Define factory test concept.
Equipment Design	1. Establish functional design satisfying allocations to include partitioning, observability, controllability, memory allocation for BIT, etc.
Assurance Engineering	1. Establish device type reliabilities and provide BITE reliability allocations. 2. Provide MTTR allocations. 3. BITE effectivity analysis (BEA) based on component failure rates and BITE fault coverage.
Integrated Logistics Support	1. Allocate field support test times. 2. Define preventive maintenance approach. 3. Determine life cycle costs. 4. Compare test approach alternatives with existing support practices.

The ease of fault isolation depends upon (1) the degree of partitioning, (2) controllability and (3) observability. These fundamental attributes must be considered throughout the design phase regardless of the level (system, subsystem, or module) or technology (digital, analog, etc.) of hardware.

3.2.1.1 Partitioning. Partitioning should be such that each function is implemented on a single replaceable unit to make fault isolation as straight forward as possible and still consistent with other requirements such as human factors, cost, reliability, etc.

If more than one function is necessary in a replaceable unit, provision should be made to allow for the independent testing of each function. In this case, electrical partitioning may be accomplished through the use of tri-state devices as illustrated in section 7. Subsequent to the optimum partitioning of the unit, the interface between one function and another must be properly designed and analyzed so that status monitoring and diagnostic data are correct and consistent between functions.

The maximum number of unit I/O pins is also a constraint on the partitioning and must be consistent with the proposed ATE.

Special test input signals, data paths, and circuitry must be included to provide the test system, whether BIT or ATE, with sufficient test points. Data paths and circuitry are also necessary to provide the test system with adequate observability for the required fault detection and isolation within the unit.

When a fault is detected, a divide-and-conquer approach for isolating to a lower level unit or component can be performed by the BIT or ATE. The proper level of partitioning, observability, and controllability will facilitate the sequencing of the BIT or ATE through a fault-isolation series of steps until the problem has been located.

The system should be partitioned so that signals at each LRU can be input and monitored independently without removing the LRUs from the system.

The capability of entering test signals into LRUs/Subsystems and monitoring their individual output without removing LRUs from the system requires considerable design forethought. It is usually paid off by reduced integration, test, debug, and repair time.

3.2.1.2 Error Budgeting. A portion of the allowable system error should be distributed to the lower level hardware to help increase the production yield and to also preclude test inconsistencies between any of the maintenance test levels. In support of this, an error budget analysis must be performed if two or more parameters contribute significantly to a higher level tolerance. The following guidelines should be observed in preparing this error budget:

- Include every parameter that contributes more than 10 percent of the specification tolerance.

- Assume a worst-case tolerance stack-up where three or fewer contributors are involved.

- Utilize ROOT SUM OF SQUARES (RSS) computation of tolerances for more than three contributors if they represent independent variables.

The error budget is then used to develop test tolerance limits for production acceptance testing. In those instances where the accuracy of the test equipment is not adequate to meet the test tolerance requirement (defined as the specification limit/measurement system accuracy) the tolerance limit contained in the Test Requirement Specification (TRS) can be adjusted as described in paragraph 3.1.3.1. Caution should be exercised because it may be more cost effective to redesign the hardware under test or to develop/obtain new test equipment than to accept the lower yields associated with tighter limits.

Since error budgets are normally set up on an RSS basis, status monitoring will look at a gross subsystem indication. Thus an out-of-spec condition may or may not be important before status monitoring calls a halt to the process, and should be analyzed carefully during allocation and design to be consistent with other requirements.

3.2.1.3 Applications of Guardbands. In setting specification design values and tolerances, the system/design/test engineers must apply a technique called guardbanding to avoid problems due to factors such as normal drift, wear, environmental effects, test equipment measurement accuracy, or noise. Figure 3-2 depicts the tolerance cone for the various levels of test that would result on a given piece of equipment when guardbands are applied.

If the specification tolerances between levels are the same (resulting in a cylindrical, rather than conical pattern), a field reject may "Retest Okay" at the depot or factory while ne'v units may fail on installation into the system. This results in large numbers of spares tied up needlessly in the file support organizations and adds significantly tc life-cycle costs.

To preclude this problem, the tolerance variation between one test level and the next should as a minimum differ by the test equipment accuracy plus a factor to cover drift due to aging and environmental conditions. The tests performed between one maintenance level and another should also be similar to minimize the No Evidence of Failure (NEOF) condition.

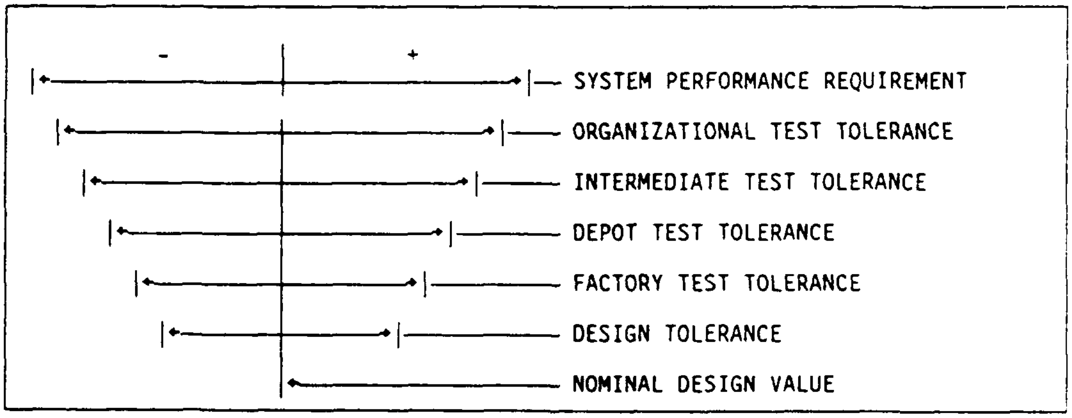

-
+
SYSTEM PERFORMANCE REQUIREMENT
ORGANIZATIONAL TEST TOLERANCE
INTERMEDIATE TEST TOLERANCE
DEPOT TEST TOLERANCE
FACTORY TEST TOLERANCE
DESIGN TOLERANCE
NOMINAL DESIGN VALUE

Figure 3-2. Test Level Tolerance Cone

3.2.1.4 Testability Tradeoffs. As a result of this interactive process, the system engineer and the testability engineer must now allocate performance and readiness parameters related to testability in order to derive firm hardware/software design specifications.

Examples of more detailed trade studies include:

- Degree of BIT versus ATE used at various maintenance levels.
- Fault resolution by BITE sensors versus diagnostic software.
- Degree of BIT self-test capability.
- Degree of on-line BIT versus off-line BIT.
- Value of failure trends analysis (fault prognostication) capability in system status monitor.

3.2.1.5 System BIT Design. (See section 4.7.1).

3.2.2 Performance Related Requirements.

- Evaluate the functional capability of the system and its sub-elements throughout a mission engagement.

- Maximize the ability of a system to re-configure (around failed elements) and sustain performance throughout a mission.

- Report fault occurrences based on a functional partitioning of the system.

3.2.3 Test Grading/BIT Effectivity. (See para. 4.9).

3.2.4 Demonstration Planning. (See para. 4.9.1).

3.3 Testability Planning Guidelines.

The following testability guidelines should be complied with prior to the starting of equipment design.

- Develop a Testability Program Plan.
- Define all testability related requirements down to the lowest applicable design level.
- Identify expected test equipment for all phases of the hardware life cycles.
- Determine the degree of BIT versus ATE to be used at the various manufacturing and maintenance levels and define the test subsystem (see section 4.0).
- Develop an error budget for all levels of hardware.
- Follow a standard such as MIL-STD-2165.

3.4 System Testability Design.

Initial requirements are established by the allocation process previously described. Iterations of this process between system and design engineers then progress as the test system definition evolves. Examples of inputs assessed by this process include:

- Test concept alternatives.
- Partitioning of test functions.
- BIT schemes to optimize visibility and observability. (See section 4.0)

Key considerations for the system engineer during concept exploration, development, and validation phases include:

- Assigning the degree of self-test capability.
- Determining the role of diagnostic software.
- Minimizing false alarms.

These factors are discussed in greater detail in the fc!!ɔwing section (see section 4, System BIT).

The following paragraphs give specific details for Testability Guidelines for System Design.

3.4.1 Connections and Cabling. The design application of system and subsystem connectors and cables affect the serviceability and testability of an electronic systerr.. In some cases, up to 90% of all system problems were caused by faulty interconnects. (Also, see section 5.2.3).

1. Interconnects can be reduced in number by use of VLSI and/or fiber-optic cables reducing overall system fault possibilities. The number of interconnects can be reduced by serializing transmitted data. Since, fiber-optic cables have a high bandwidth, more data can be serialized than in a conventional cable.

2. Connector and wire types should be standardized to improve test and logistic conditions.

   Avionic and ground systems generally incorrorate "standard" connectors, but the number of "different" standard connectors should be kept small. Use the same connector type keyed differently where possible.

3. Provide effective connector keying, color coding, and marking to prevent mismatching.

   Defeatable keying on LRU connectors reduce the number of unique interface adapters needed for a specific ATE.

4. Provide adequate clearance around connectors for engagement/disengagement of cables and proper connector orientation in 3 minutes or less.

   Removing and replacing cables (neatly bundled) in less than or equal to 3 minutes can be accomplished with good mechanical design of system interconnections by using quick release cables and not having to remove other cables to get to any specific cable.

   Remember also to provide adequate space for cables, including sleeving and tie-downs, and adequate service loops for ease of assembly/disassembly.

5. Label, and where possible color code, each wire in a harness or cable to facilitate tracking from origin to termination.

   Systems providing any where from a half a dozen to hundreds of cables become impossible to integrate, test, debug, or repair without each end of the cable clearly marked (and keyed) as to the exact LRU and connector number it is to be attached to. Marking the cable designator on the cable along with bar codes is also recommended.

6. Standardize connector pin assignments for power, ground, and other frequently used signals.

7. All LRU/subsystem critical nodes (and or test points) need to be accessible from a connector to prevent need for internal LRU probing or access.

8. Avoid hidden cables.

   Visually inspecting and tracing all assembly cables rather than having hidden cables (such as behind other cables or even LRUs) allows for a quick system and cable integrity check which aids in overall system integrity and debug. This also implies quick access for manipulative actions.

9. Provide at least 10 percent spare wires on all multi-conductor cables. This is especially true for cables which are used in between bulkheads connecting LRUs dozens of feet apart. A break in any connector allows a quick rewiring at each LRU end rather than trying to pull out a 150 foot multi-conductor cable.

10. Avoid right angle connector shells. If used, pay attention to each cable lay. If cable lay is not watched, a right angle connector shell can provide unnecessary cable wear on individual conductors lowering cable life.

3.4.2 Power. Power supplies are usually standardized by such MIL-STDs as 1760B and 465B. Avionic power supplies usually run at 400 Hz as opposed to the usual 60 Hz for ground systems. Avionic systems usually are ± 40 V, ± 28 V, ±15 V, etc., while ground systems run at 220 Vac, 115 Vac, +28 V, ± 15 VDC, etc.

- Using standard power on avionic and ground systems, makes interconnections to standard ATE much easier reducing test times and cost of not having to design power adapter circuitry.

- Disconnecting the high power section from the system and then being able to check at other (low power) LRUs provides much better safety to the test engineer, especially if the interlock problems can be solved.

- Also on power failure of the main system power supplies, system design should be done in such a way that one is able to quickly disconnect power cables and apply external power supply signal connections.

For high power testability design, see Section 14.

3.4.3 Computer/Controller, Interconnecting Buses and Software. More and more "Systems" are controlled by some form of computer control using interconnect buses to connect LRUs. Testability guidelines are as follows:

- Be able to reset the system at any time either remotely or by means of a reset switch or push-button (in case it should get "hung up").

  Computers occasionally "hang up" due to any of many reasons including faulty software (prevalent in very large systems). Provisions have to made to bypass computer control and regain manual control or the system may be lost.

- Provide direct access to address/data buses so ATE can read data directly from the system and exercise individual components.

  Standard test and maintenance buses (such as IEEE-STD 1149.1) accessible through a test connector greatly simplifies system troubleshooting by supplying access to all faults through the connector.

- Use standard communication signals between systems, subsystems, and LRUs (such as 1553B, an avionic requirement) so dissimilar systems and all ATE with 1553B capability can be hooked together, without design of costly adapters.

- Divide system software into common software module/structures by system function to greatly enhance testability of individual functions for both software and hardware.

- Employ higher order software languages.

  Employing a higher order software language in a system make it much easier to integrate, test, and debug since the test engineer can easily interface to the controller through a keyboard.

- Use a standard like the ARINC Communications and Reporting Systems for remote diagnostic/maintenance to makes life easier for the test engineer and requires less customized ATE equipment for test (especially for satellites, etc.).

  Often critical functions will require redundant circuits for fault tolerance. These redundant units must be tested independently so that faults can be isolated to one of the redundant circuits.

3.4.4 System Test Points. Test points are not usually related to systems, but are often provided in system control panels to check out remote system LRUs from a central location.

- For system test, test points for I/O and readouts should be in close proximity to each other so that one test engineer can perform a test while monitoring the readouts. If more than one engineer is required, test cost will escalate.

- Provide system test points with contamination cover.

  System test points without protective covers are prone to system contamination. Also, depending on contamination type, test points can become functionally useless with time reducing overall system testability.

- Design test points to not interfere with tested signal during integration.

  Incorrect design of test points (without buffer circuitry, i.e., a resister, etc) can lead to disastrous effects to main circuitry.

  Incorporate standard impedance level at test points so test equipment can access these test points directly without need of additional circuitry (such as 50, 75, 130 ohms, or greater than 130 Meg. ohms).

3.4.5 Mechanical Guidelines;. Many of the general mechanical guidelines for modules also apply to systems (reference section 6). Much time is usually lost removing the LRU after a system problem has been diagnosed to a subsystem or LRU.

- Design the system such that an LRU can be replaced in ≤ 30 minutes.

  Replacing LRUs/Subsystems in ≤ 30 minutes (without special tools) is a good rule of thumb easily accomplished with good mechanical design for testability and repair (such as utilizing fewer screws, 1/4 turn screws, and not hard-wiring removable covers.

- Avoid manual adjustments at the system level.

  Manual system interactions such as 'select at test' and manual adjustments slow down overall system test, debug, and repair (costing more time and money).

LRUs/Sub-systems should be mounted on drawer slides or extender racks to provide easier accessibility during integration, testing, debug, and repair of these UUT, especially when the LRU is still in the system.

- Use a modular system design (see MIL-STD-2076, AFLC/AFSCP 800-39, 3960-90).

  Modular system design means that each subassembly is designed as a functionally complete entity. If this were not the case, then when a subassembly was removed for testing, ATE would need custom circuitry to simulate missing functions.

- Clearly mark all subsystems/LRUs.

  When a system contains multiple LRUs or subsystems which are not clearly marked with ID numbers, generic English identifiers, and location reference designators, then sy stem integration, test, debug, and repair can become a nightmare if not impossible.

3.4.6 System Safety Considerations. System operators and test personnel safety is of prime concern during design of a system for testability and outweighs all other testability requirements.

- Clearly mark hazardous or hazard emitting systems both in English and in'*national symbols when requiring system covers to be taken off just betore testing or a mission.

- Provide fire/smoke/hazard Detectors.

  Fire/smoke detectors and sprinkler systems protect not only the system but also the test engineer during integration, test, and debug.

- Au safety and arming devices should be provided with visual/audible alarm plus single switch deactivation,

  Missiles contain self destruct mechanisms on adjustable time fuzes. It is absolutely essential that these self destruct sequences are not only available through a special multi-sequence code to prevent accidental turn-on during test, but include a visual/audible warning on turn-on, and a single switch deactivation for both manual and remote service.

- Provide all automatic override operator monitors with a visual or audible alarm.

  Complex systems contain "operator monitor" to take evasive or other action if operator fails to do so in a given amount of time after warning sounds.(such situations arise in battle: approaching obstructions, altitude too low, approaching threat (missile)). Test engineers need audible/visual warning before one of these monitors engages, for safety reasons.

- Provide Battle Shorts with audible/visual alarms.

  Often systems will include a 'battle short' switch which allows a system to continue running despite catastrophic internal problems which can result in fires and even explosions. Using an audible and visual display to warn the test engineer it has been engaged, is absolutely necessary.

- Any explosive circuitry should contain a code sequence to activate it and a deactivation switch in case it is accidentally activated.

3.4.7 System Testability Design Summary. To insure compatibility with all present and future USAF ATE and greatly reduce the need for custom ATE, use MIL-STD-1760. It is used on many avionic platforms including: B1-1, B-52, F-15, F-16 Programs. It provides I/O standards including plug/connector, socket, and pin connection types, 3 phase AC power, 2 independent 28 volt power supplies, and a future requirement of two fiber-optic connectors.

Systems capable of providing their own stimulation by being functionally independent require less test equipment (i.e, no external stimulation is required and ATE does not have to provide for missing functions). This makes systems easier to test by fault isolating to one function.

1. Long test times (≥ 10 minutes) usually cause a system to heat up considerably and are not recommended without auxiliary temperature monitors and cooling equipment available. Also, if a system has to warm up for more than 10 minutes each time it is shutdown for any reason during test, test time can increase to the point of impracticality.

2. For remote systems, provide factory "mockup" systems.

   Often inaccessible systems develop specific faults that cannot be diagnosed without access to an identical "non-flight" system in the factory. The non-flight systems can be used to simulate the error and debug a problem before a line of action can be recommended.

3. Provide easy access to subsystem LRU backplane.

   A good way to gain access to an entire LRU backplane is through an empty card slot, if any are available (other than all operational test points coming out through a test connector).

4. Provide quick access to removable items.

   When fuses, transient protectors (for lighting strikes), desiccants, etc. are quickly accessible without having to remove LRU covers, over-all test times can be reduced.

5. Avoid custom design systems when commercial equipments are available.

   Use standard of-the-shelf commercially available electronic modules such as power supplies and controllers. They are cheaper, since spares are available that can simply be interchanged at any hint of trouble. Custom design units need to go through long debug times.

6. Provide ground terminals for system test.

   All LRU/subsystems need good measurement instrument ground terminals on their structures, otherwise, it is difficult to know whether good contact is being made.

7. Avoid filling a system with gel, inert gas, or even pressuring with gas. It can greatly increase integration, test, debug and repair times from days to months (if it can be tested at all).

8. Avoid needing a clean room etc. to test a system/subsystem, by clever design. Requiring a laminar flow bench or a clean room (class 100 to 100,000) can greatly complicate system integration, test, debug and repair times (clean rooms abound with hidden costs). Systems can be designed to minimize or eliminate these requirements.

9. Avoid need for "state-of-the-art" ATE. A system should be designed so that it can be tested with simple of-the-shelf "commercial" ATE. "State-of-the-art " ATE usually is very expensive.

10. Provide testability coverage to at least 90%, or greater, of all possible faults. For a system/subsystem or LRU to provide isolation to 90%, or greater, of all possible faults to the next level of disassembly gives an excellent coverage and is usually the minimum required in DoD contracts.

11. Provide for an on line "Expert Diagnostic System" through the system controller. Availability of an "Expert System" for system diagnostics greatly simplifies the test, debug and repair procedure saving considerable time, effort, and cost.

12. Be able to break all system feedback loops. System level feedback loops need to be broken and controllable by ATE to isolate problem to individual sections within feedback loops.

13. Provide redundant circuits for critical system functions. By employing redundant circuits for critical system functions, the off line sections can be tested with no system interruption of main functions. The system can usually switch in very short time allowing other circuits to be tested. This redundant circuit can aid in overall system testability.

14. Provide system access to any circuitry employing a scan testability technique. Scan techniques (although meant for IC and/or CCA checks) can also be employed in system checks by allowing a user to access internal registers and signals. See section 11 for more information.

15. Provide system "self" calibration. Automatic self calibration of system functions, especially to government calibrations standards, verifies accuracy of system measurements and does not require external calibration equipment.

16. Provide all necessary documentation and specifications for system testing. A total specification and documents package needs to be available for maximum expediency of integrating, testing, debugging, and repairing systems. (see section 2).

SECTION 4. SYSTEM/SUBSYSTEM BUILT-IN TE⌐⌐ (BIT) GUIDELINES

4.0 OVERVIEW.

Avionic and ground systems are becoming more complex. A typical system may contain dozens of subsystems (or LRUs) incorporating hundreds of circuit cards with thousands of VLSI circuits including more than one hundred microprocessors/controllers all connected by many miles of cables. These systems are beginning to require more and more support equipment .

To reduce manning and skill level of the system operators and maintenance/test personnel, the systems themselves must have designed into them a high level of "system self-test " achieved through Built-in Test Equipment (BITE) performing Built in Test (BIT); also . sometimes called Built-in Self Test (BIST). BITE can be identified as a component or group of components including re-workable stand alone test equipment modules, and unique circuits within functional modules. (For information on module level BIT, see section 6).

BITE (performing BIT) should be designed into a system so that the BITE does not effect the operation of the prime avionic/ground function and that the function could continue with no BITE present.

System Level BIT can require as much as one third of a total system "Real Estate" circuitry which includes area and weight not to mention additional power requirements.

4.1 System BIT Advantages for the U.S. Defense Dept. Maintenance Levels.

Avionic/Ground Systems have historically been divided into 3 levels of maintenance.

- Organization Maintenance Level
- Intermediate Maintenance Level
- Depot Maintenance

The present trend for the 90's is to reduce this to two levels: the organizational and the depot level.

4.1.1 Organizational Maintenance Level. BITE/BIT is used predominantly at the organizational level for systems (reference RADC-TR-87-55). BITE/BIT gives the operator confidence that the system can or cannot perform a particular mission.

At this level, BIT improves operational readiness by reducing down time, i.e., reducing Mean Time to Repair (MTTR) and by reducing support resources such as:

- skill level needed to isolate and replace modules identified by BITE/BIT and

- the size of the inventory required to support module replacement

This is all achieved since BIT and fault isolation is integral to the system design. In many cases, module level BIT can be exercised at the system level and again at the organizational repair point to verify the module indictment of the system test.

4.1.2 Depot Maintenance Level. Module level BIT in conjunction with external test equipment is used for further fault isolation at the Depot. This will be discussed in more detail in section 6.

4.1.3 Actual BITE/BIT Penalties. BITE/BIT overhead circuitry for the older 3-level maintenance approach can be as low as 3% for a simple "end-to-end" test of an Intercom to almost 40% overhead circuitry for extensive BITE/BIT needed to achieve a 98% fault isolation down to one LRU for a complex ground based Radar System.

4.2 System Self-Test.

System self-test can be broken down into two large categories:

- Central Integrated Test System (CITS).
- System Integrated Test (SIT).

4.2.1 Central Integrated Test System. CITS is a system self-test and maintenance approach using a dedicated centralized computer controlled Airborne/Ground Test system which is an integral part of the Prime system. Such a system is used in the B-1 bomber (see figure 4.1). Here a dedicated test diagnostic control console/CRT is available between the two rear seat pilots. This console monitors mechanical system conditions including battle damage.

4.2.2 System Integrated Test. SIT is the other system self-test and maintenance approach in which data is gathered using BITs existing in individual subsystems/LRUs. A computer not primarily dedicated to system self-test may store and compare these data outputs between subsystems on a limited basis.

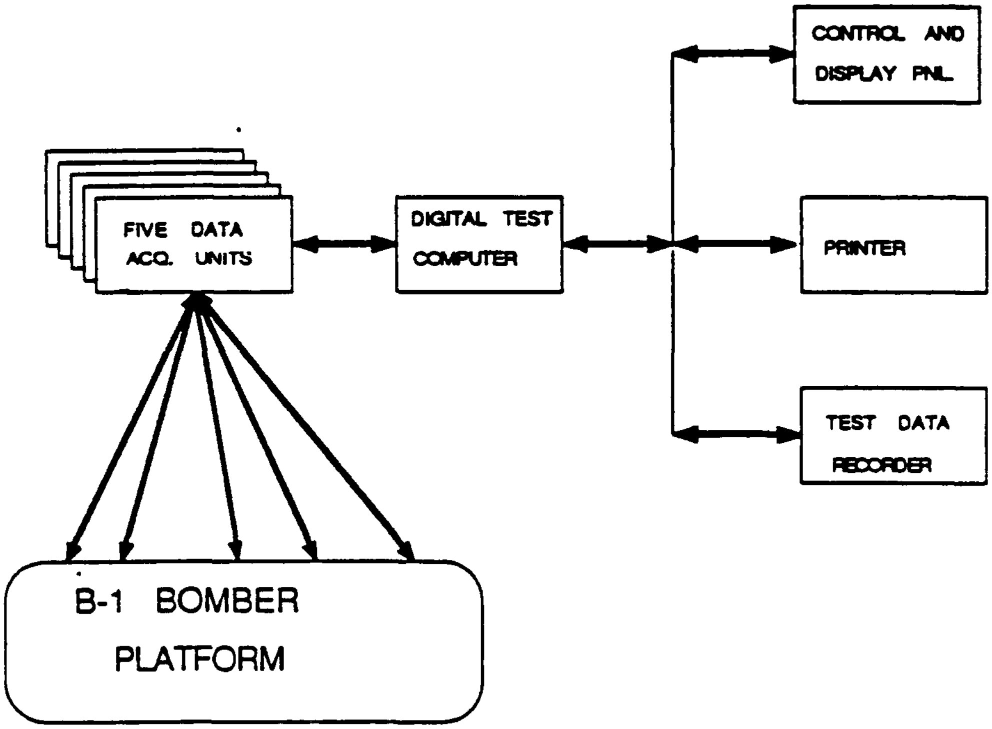
4.2.3 BIT Classification. The above two categories of self test may utilize one or more of the following classes of BIT.

1. On-line (active) BIT;
   Background non-interference testing while main system function is on.

2. On-line (passive) BIT;
   BIT on demand (a push of a button) may interfere with main system function.

3. Off line BIT ;
   Such extensive BIT as to require main system function to stop.

These will be discussed further in paragraph 4.6.



B-1 BOMBER SUBSYSTEMS CHECKED BY C.I.T.S.

FUEL SYSTEM
ENGINES
ENGINE THRUST CONT
ENGINE ANTI-ICING
FIRE PROTECT.
PITCH
ROLL
YAW
AIR DATA SYSTEM
GYRO STAB SYS
WING SWEEP
FLAPS AND SLATS
STRUCTURAL MODE CONT
SPOILERS
LAUNCHERS, RACKS

FL DIRECTOR CMPTR
LANDING GEAR & DECEL
ELEC POWER DIST
E-MUX
HYD POWER
SEC POWER
BLEED AIR
AIR COND/PRESS
ENVIRON PROTECT.
ESCAPE SYSTEM
LIFE SUPPORT
ENGINE INSTR
AIR INDUCTION CONT.

Figure 4-1. Example of B-1 Bomber Weapons System Employing CITS

4.3 System BITE Functional Characteristics.

System BITE functions designed into a system should incorporate the following three (3) general suggestions:

- Failure of BITE circuitry should not effect system performance.
- BITE circuit reliability should greatly exceed hardware being tested.
- "Simple" BITE circuits should monitor and detect 85%, or greater of all the predicted failures of the system being monitored & tested.

4.4 System BIT Functional Characteristics.

BIT within a system performs three related basic functions:

- System monitoring.
- System checkout.
- Fault isolation to an LRU.

Fault isolation, of the three, is the most complex.

4.5 System BITE/BIT Software/Hardware Tradeoffs.

4.5.1 Software BIT Advantages. Software implies hardware in the form of a computer (or controllers) and software. The advantages are:

- Offers ability to renrogram different BIT during system modification.
- More comprehensive; using a fixed amount of hardware.
- Provide input stimuli and monitoring of the outputs of the system under test, especially for cables between subsystems.
- Provide diagnostics for a functional area fault isolation.
- Store BIT threshold (value which defines if a BIT measurement is a fault) incorporated in software.

Cost of applying software BIT can be reduced to a minimum, for hardware, if the system computer/controller shares operational and test functions. When system computer resources are not available, dedicated computers have to be provided much as in the CITS testability approach discussed earlier.

4.5.2 Hardware BIT advantages. This type of BIT is very useful in areas of signal format transformation (A to D and D to A). The greatest value for this type of BIT is where software cannot be used efficiently. This includes:

- Areas which are not controlled by a computer such as a power supply (using visual BIT indicator).
- Systems which have computer control but have no memory left for application to test programs and only minimal real estate for test circuitry.

4.6 On-Line (Active/Passive) Versus Off-Line BIT.

On-line active and passive BIT, and Off-line BIT was defined in paragraph 4.2.3. The difference between the two is discussed in the next two paragraphs.

4.6.1 On-Line BIT (Active and Passive). On-line BIT in system testing usually results in immediate detection of critical system malfunctions.

- Always maximize the amount of on-line active BIT as long as it does not interfere with functional system processing or required processing time.

- BIST to be automatically run as an on-line active BIT and in some cases activated on demand by off-line passive BIT (see para. 4.6.1.1). It should also be able to be activated on demand by an operator.

4.6.1.1 On-Line Passive BIT. Passive On-line BIT (BIT on demand), causes minimal interruption of normal functions and may be acceptable in certain systems (Radar systems, etc.), but in others could disrupt mission critical functions (such as auto pilots). Often on-line active BIT is a subset of user demanded passive BIT.

4.6.2 Off-Line BIT. Off-line BIT is used mainly after a system malfunction has occurred during On-line BIT and it is necessary to perform such intensive BIT testing as to require system prime function to be shut down until testing is complete.

System specification requirements in regards to system mission dictates the best combination of On-Line/Off-Line BIT for a given design.

4.6.3 Inductive/Deductive BIT. Inductive and deductive BIT techniques are useful in systems that have limited available real estate, weight, size, and power.

4.6.3.1 Inductive BIT (IB). IB is used to induce that a single function is within its stated limits, by the fact that test functions which generate these untested functions are within stated tolerance limits themselves.

4.6.3.2 Deductive BIT (DB). DB is used to deduce that when a tested function is within its tolerance limits all variables used to generate this function must also be in their respective limits. In other words if a radar system output is measured normal, the assumption can be made that transmitter, waveguides, cables and power supplies must be functioning correctly.

These two methods (IB+DB), although necessary in diagnosing problems in systems, do not provide as much detail as off-line BIT and are subject to large FALSE ALARM RATES.

4.7 BITE/BIT Design Considerations, Suggestions, and Definitions.

As mentioned in section 3, key considerations for the system engineer during concept exploration, design, development, and validation phases include:

- Assigning the degree of self-test capability. (See section 4.7.1).
- Minimizing false alarms. (See section 4.7.4).
- Determining the role of diagnostic software. (See section 4.8).

These factors are discussed in greater detail in the following paragraphs.

4.7.1 Configure Optimum System BIT Design. In order to configure an optimum BIT design and assign the degree of SELF TEST capability, various inputs are required.

1. Worst- case stress analysis must be available to ensure that any circuit failures induced by temperature extremes, end-of-life tolerances, combinations of component tolerances and power supply variations are detected and that an excessive number of false alarms are avoided.

2. BIT system thresholds must be consistent with lower level test specifications to prevent excessive No Evidence of Failure(s) (NEOFs) from occurring.

3. Reliability predictions must be performed so that high failure rate items can be identified. In conjunction with the prediction, a Failure Mode and Effects Analysis (FMEA) should be done to ensure that malfunctions will not adversely affect other units and to determine the exact level of BIT achieved. The FMEAs are derived from functional flow diagrams, schematics, and timing sequence diagrams, which are analyzed for various failure modes (Reference "BIT Verification Techniques" RADC-TR-86-241).

4. A list of all components, their failure modes, and associated failure rates is systematically developed. From this list, high failure probability components are chosen as BIT interrogation candidates.

5. As was shown in the System Chapter (section 3), On-line monitoring, in general, is the most desirable mode of operation and is dictated by the prime system and mission needs and this requires tradeoffs in cost, technical impact on the design, and the operational requirements for the mission. A major determinant in selecting candidate test subsystems is the required mean corrective maintenance time (M_{ct}).

   A major item in the M_{ct} calculation is the time to disassemble, interchange, reassemble, and check out the system. When this information is known, the time remaining in the M_{ct} calculation for isolation and localization is available.

Prime equipment can be field tested with BIT or ATE. However, for systems with digital processing capability, the hardware BIT concept is the more cost-effective approach. The BIT should have the capability to not only detect subsystem faults and isolate to one subsystem module or group of modules, but also should provide aid in isolating to a specific faulty component for use during production or CCA repair.

The degree of fielded off-line testing will largely depend on decisions regarding specific maintenance levels and locations.

Once all of these decisions have been made, it can be determined what level of BIT is required to locate the malfunction to a functional area and how small that functional area should be.

The following sections show how the system level of BIT chosen can be described with relation to this overall system:

4.7.1.1 Readiness Requirements. Readiness is a generalized concept defined by the states of an operating system. All readiness parameters quantified in system design requirements can be related to availability, which is defined in MIL-STD-721B as "a measure of the degree to which an item is in the operable and committable state at the start of a mission, when the mission is called for at an unknown point in time."

4.7.1.2 Fault Coverage. The fault coverage parameter relates to the ability of the test system to detect faults. It is evaluated by determining the ratio of the probability of occurrence of detectable faults to that of total faults. Implied in the definition is a categorization of fault criticalities (degree of system degradation as a result of the fault). Care must be taken to define a criticality range that is suitable for performance and maintenance functions.

4.7.1.3 Fault Localization. Fault localization relates to the ability of the test system to identify specific hardware groups that do not meet performance specifications. Localization is thought of as the general process of isolating faults in a system. A common measure associated with the localization process is % detection, defined as 100 times the ratio of the number of isolations (to replaceable or repairable end items) to the number of faults detectable by the test system.

4.7.1.4 Fault Resolution. The fault resolution parameter measures the ability of the test system to isolate faults within an assigned ambiguity level. An example of the use of fault resolution in specifications is requiring that the test system isolate faults to not more than five field replaceable circuit cards. An additional part of this requirement could be that an average fault resolution must be two circuit cards or less.

4.7.2 Fault Detection Time. Fault detection time is the time that elapses between the occurrence of a fault and the detection of that fault by the test system and subsequent indication at the man/machine interface.

4.7.3 BIT False Alarm Rate (False Failure Annunciation Rate). The false alarm rate is the percentage of test system fault reports that are erroneous. This parameter is the result of effects categorized as follows:

> Category I - a fault report when the tested equipment has not, in fact, failed, possibly due to system noise, or BIT circuit failure.
>
> Category II - improper isolation of an equipment fault due to a test system error. This results when a fault-free unit is identified as no-go when the fault was in another unit.

An example of false alarm in a real life system is again the B-1 Bomber. Early production bombers were plagued by so many BIT false alarm errors that pilots routinely flew their missions totally ignoring the BIT failures reported. Most of these BIT errors could not be repeated when the bomber landed. Causes were attributed to hardware and software design problems of BIT circuitry in the CITS. In these cases, investigation into system noise and the way test tolerances and measurements were made may reveal the problem.

4.7.4 BIT False Alarm Rate Reduction Techniques. BIT for an electronic system can be thought of as consisting of system-level and unit-level tests. When no-go indications are present with current BIT designs, a common basis for localizing faults to the unit that should be replaced is to use logical relationships among the system-level no-gos.

This approach is frequently ineffective, particularly in instances where BIT indications imply the existence of multiple faults. Fault isolation logic that does not apply to the conditions existing at the time of test performance results in Category II BIT false alarms (the fault exists, but is incorrectly isolated).

BIT should be decentralized to reduce ambiguity in fault localization. This concept sometimes called federated BIT, will also help reduce the cost of subsystem test during production.

Federated BIT (the cure for Category II BIT false alarms) puts the BIT tests "in the box." Under these conditions, when a no-go is present, the location of the fault is unmistakable. The federated BIT concept is to have BIT comprised primarily of unit-level tests (some system-level tests are still needed to verify certain functions). Under these conditions, most faults indicated as present will be correctly localized to the faulty unit.

4.7.5 Summary of False BIT Alarms (FBA). FBAs can generally be attributed to transient or temporary conditions involving the ambient environment, electrical noise, or human error. Some examples are:

1. Operator error - The operator of the system containing the unit under test incorrectly used the unit, incorrectly interpreted unit behavior, or both; the operator erroneously perceived and reported a malfunction, and no malfunction subsequently can be duplicated by maintenance personnel.

2. Latent Built-In Test Design Error Manifestation - AS a product of coincidence, an appropriate sequence of events occurs that cause a latent BIT design error to manifest itself; maintenance personnel subsequently cannot duplicate the sequence of events that precipitates the error manifestation.

3. Environmentally induced BIT error - Environmental conditions such as, vibrations, pressure and temperature, cause transient behavior in the BIT system such that a malfunction is erroneously reported; subsequently maintenance personnel cannot reproduce the conditions that cause the transient behavior.

4. BIT Transient Failure - Component degradation in the BIT system causes a failure of a transient nature, resulting in an erroneous report of a malfunction in the host system, and the transient behavior subsequently cannot reproduce the conditions that caused the transient behavior.

5. BIT Hard Failure - A failure occurs in a BIT subsystem, a malfunction of a subsystem is reported, and the suspect system is not host to the accusing BIT; maintenance personnel subsequently verify the unit to be good.

6. Latent Design Error Manifestation - As a product of coincidence, an appropriate sequence of events occurs that cause a latent design error in a system to manifest itself; subsequently, maintenance personnel cannot duplicate the sequence of events that precipitates the error manifestation.

7. Transient Failure - Component degradation in the system causes a failure of a transient nature, resulting in a report of a malfunction of the system; the transient behavior subsequently is not exhibited during testing by maintenance personnel.

8. Environmentally Induced Functional Error - Environmental conditions such as, vibrations, pressure and temperature, cause transient behavior in the BIT system such that a malfunction is erroneously reported; subsequently maintenance personnel cannot reproduce the conditions that cause the transient behavior.

9. Organizational Maintenance Level (OML) Test Equipment Error - An error in the test equipment used at the OML identifies a good unit under test as being faulty; subsequent maintenance levels verify that the suspect unit is not faulty.

10. Human Error at OML - A human error at the OML results in identifying a good unit under test as faulty; subsequent maintenance levels verify that the suspect unit is not faulty.

11. Depot Level for Shop Test Equipment Failure - An error in the test equipment used at the shop level identifies a faulty unit under test as being good.

12. Human Error at Shop Level - A human error at the shop level results in the identification of a faulty unit under test as being good.

False BIT alarms have been previously recorded in many avionic and ground systems; but, then were unable to be duplicated through even extensive testing. These false BIT alarms are known as Can Not Duplicate (CND) failures.

4.7.6 Smart BIT (reference: RADC-TR-85-198). "Smart" BIT is a term given to BIT circuitry in a system LRU which includes dedicated processor/memory to make on-board decisions about the validity of BIT results. In this way it can reduce false alarm rates and improve overall module/system readiness.

DoD demonstrations have shown that "Smart" BIT can identify faults that were not detected by conventional BIT.

Smart BIT also improves fault type classification and reduces the number of ambiguous groups.

Finally, when an LRU/Module/System includes "Smart" BIT, UUT problems can be solved with a Modem over telephone lines by a large central computer system which can run countless fault simulations and send results to remote UUT sites (Ref. MIL-STD-2084).

The one large drawback for "Smart" BIT is that it uses a good deal more physical real estate, or software/firmware memory. This also may mean increased power needs and heat dissipation. All of which may not be available on LRUs/modules/systems, especially in avionics.

4.7.6.1 BIT Data Recording. Under the assumption that BIT is implemented by use of continuous monitoring, there is a need for a capability to record the successive results of this monitoring for later evaluation.

The quantity of test result data from continuous monitoring is potentially enormous. However, the amount of data that is recorded can be kept to manageable size by:

- Limiting the number of signals that are monitored.
- Limiting the maximum sampling rate.
- Reducing the time span over which data is accumulated.
- Restricting the type of data accumulated.
- Using computational techniques which do not require storage of old input data. (For example, mean values and standard deviations can be based on the results obtained at the last sample time and the current input only.)

4.7.6.2 BIT Data Filtering. There is a need to summarize and evaluate recorded BIT data so that the results can be used by equipment operators (to decide how to use BIT to verify mission functions) and maintenance personnel (to decide what maintenance, if any, is required).

Recorded BIT data must be summarized and evaluated in such a way that the results serve the needs of both operators and maintenance personnel. How this is accomplished depends upon the specific characteristics of the BIT data that is stored. Stored data may be in one of the following forms:

- Raw values obtained each time a BIT-monitored signal is sampled.
- Failure rate
- Sampled signal data from which mean and standard deviation values can be calculated.

To meet the needs of a system operator, the stored BIT data must be retrieved and summarized in order to provide the operator with real-time information concerning the status of the equipment. If the equipment has a malfunction, the operator must be told which equipment modes, if any, are still operative. Equipment status information must be continually updated for the operator from the start of a mission until its completion.

To meet the needs of maintenance personnel, the stored BIT data must be retrieved and summarized after a given mission and, if desired, stored for subsequent use. The process of BIT Data Filtering must answer the following questions for maintenance personnel:

- Does the system require maintenance?
- If so, which unit of the system is faulty?

4.8 General System BIT Design Guidelines.

Listed are guidelines for developing BIT test schemes, capabilities, and diagnostics for both circuitry and software controllers.

1. Mission critical functions should be monitored by BIT.

2. BIT tolerances should be set to maximize fault detection and minimize false alarm rate in the expected operating environment.

3. BIT fault detectors should be designed to accommodate the needs of operator maintenance personnel.

4. Concurrent BIT should be used to monitor system critical functions. Fault masking resulting from the use of redundant circuitry must be minimized.

5. BIT reliability as a design goal should be an order of magnitude higher than the circuitry it is monitoring. If the BIT circuitry has a relatively high failure rate,then the system reliability may be noticeably affected.

6. BIT must be designed to be fail-safe. A failure in the BIT circuitry itself or any of the interconnects (including inadvertent omission of a cable) should result in a fault indication.

7. Estimated system life cycle cost data should be utilized to optimize test/availability and final production costs of system.

8. In the area of software design and test responsibility, the responsibility for the design and development of verification testing of an end item (e.g., digital filter) should reside with the same engineer(s).

9. Use CITS self-test wherever possible.

10. Use SITs only when CITS is not economical or otherwise possible.

11. Stimuli and response data for each diagnostic test must be defined at the system/subsystem level. The same data should be planned for use both in factory testing as well as in field maintenance of the equipment. This data minimizes the amount of unique software to be written.

12. Provide for manual control of test sequences, so that the test can be selected individually, and appropriate test combinations can be executed at the operator's discretion. Also manual control is needed to abort a test at any time.

13. The effectiveness of a diagnostic program is highly dependent on the types and quality of BITE circuitry, BIT, and on the quantity and strategic placement of monitored test points within the equipment. These test points must be planned for and provided for by the equipment design engineers early in the design phase.

14. Fault Isolation. The diagnostic test for all units within a system/subsystem shall assess the unit's operability and isolate failures to replaceable items.

Some basic guidelines for fault isolation considerations of diagnostic tests include:

- Designing each test so that it will:
  - Execute independently of all other tests.
  - Diagnose a functional portion of the unit.
  - Be initiated upon completion of higher priority predecessor tests for this unit.
- Designing fault isolation routines so that the results of only one independent test have to be analyzed. If fault isolation requires analysis of the results, the last test in the sequence shall analyze all the results.
- Having each independent unit test provide both a GO/NO-GO status indication and fault isolation to the cause of the failure.
- Wherever possible, make each test capable of being terminated prior to completion and then being re-initiated at its start point automatically or as an operator option.
- Designing the unit tests so that they can accommodate the following subsystem response modes:
  - Incorrect response from the subsystem, including no response conditions.
  - Inconsistent response conditions.
  - Unexpected conditions.
- Designing all software so that it is structured by test priority. The test software should take advantage of both subroutine constructs for all message outputs and of failure dictionaries which identify the location of the most likely failed replaceable unit

15. System software programs should include a bootstrap or equivalent function to establish a Minimum Working Instruction Set (MWIS). From this MWIS other instructions can be established as working correctly, in this way verifying an entire system controller instruction set.

16. BIT circuitry provided to establish computer/controller activity (such as a watchdog timer).

17. Supply a system control panel lamp check button to be used before system operation or system test.

18. Use standardized BIT structures in both hardware and software (as BIT modules and algorithms) to minimize overhead BIT costs.

19. In an Airborne Avionics System, mission critical faults should be sent to a pilots "head-up" display along with an audible alarm. In this way the pilot does not have to take his eyes off of the outside world to check for critical system and/or mission threatening problems.

20. Be sure that system user manuals include instructions for faults not covered by BIT such as, system will not power up or system is being used in an incorrect environment such as, at the wrong altitude, etc.

21. Ground maintenance BIT (also referred to as active on-line, or even off-line BIT) should have a special switch on the system control panel to allow for manual override of the BIT routines. In this way critical system functions can be restarted when needed. An example would be to inhibit an off-line test BIT being run on a Air Force fighter plane, when the test needs to be suddenly halted due to an unforeseen mission which requires aircraft readiness.

22. All self-test routines should be stored separately from functional firmware so that problems in test software can not corrupt system functional firmware.

23. For high power systems/subsystems, high power sections should be interlocked with visual/audible BIT to only allow system turn on when it is safe to do so for both test personnel and system safety. (See section 14).

24. BIT calibration for a large system should always be bundled under computer control with manual intervention possible.

25. Before any BIT is run on a system, BIT should check itself first for BIT circuitry integrity before main system self test starts (like self test on "power up").

26. For easy repair of system faults, system BIT diagnostic failures should be reported in clear English and not in code numbers or turned on lights

27. BIT circuitry should be located on the level of subsystem that it tests. This makes it easier to test and repair the system when it is removed from the main system since BIT will still be located on it.

28. Keep system testable ambiguity groups to as small a size as economically possible (ideally, one replaceable serviceable SRU per fault).

29. Use of a BIT building block approach is another method that can be used if enough system real estate is available for its implementation.

30. Fault tolerant redundant circuits each need a full complement of some type of BIT technique.

4.9 Test Grading System BIT Effectivity.

Test grading of the BIT effectiveness is the responsibility of the system engineer, the design engineer, and the testability engineer who must devise a plan for quantitatively grading the percent of faults that are detected and isolated.

4.9.1 Demonstration Planning. A demonstration must be performed to verify the achievement of specified testability parameters on major end items using the anticipated test equipment, test software, and test documentation. This demonstration, usually accomplished using contractor personnel and facilities, is monitored by the procuring agency.

The procedure includes the introduction of actual failures into equipment for the verification of BIT, test software, and maintenance error dictionaries. The plan should be developed by the assigned Testability Engineer, the Design Engineer and the System Engineer. Prior to the actual demonstration testing, faults should be inserted into the hardware to pre-verify testability performance.

4.10 System BIT Summary.

It should be noted that some types of BIT circuitry which may be ideal for one system may be unacceptable for other systems depending on the Prime System requirements.

For instance, a planetary probe or satellite will need BIT distributed throughout the entire system, while a ground based systᵣₘ like a ʳadar or even a land vehicle could benefit from leaving all BIT control circuits on one circuit card which could be easily removed and replaced. (Item 27 of para. 4.8 is the preferred procedure)

Finally, in larger systems such as the B-1 bomber or a ground based radar complex, it is suggested that many types of BIT request levels are available from a central console. In this way a Top Level BIT test would simply give a system operator a quick check of the functionality of the entire system, in a short amount of time.

For instance a pilot, after having been hit by anti-aircraft fire, may want to quickly asses if the plane can still continue with this mission, the mission needs to be abandoned, or the pilot needs to eject, since the plaₙe is no longer safely flyable. A "top level" On-Line Active BIT check can provide these answers, and if so, action required should be stated in clear English.

A lower level On-line Active BIT check could check individual troublesome systems. Examples are checking a weapons platform on a plane, or one of its four engines, etc..

A bottom line (On-Line Active) request for total system BIT check might only be done once before a system mission. It can take anywhere from a few seconds to several hours depending on system size and BIT complexity.

The above concept, in the preceding paragraphs, is an example of "Smart" BIT where BIT differentiates between "Real" and "False alarm" system failures. The Smart BIT system reports the failures and their causes to the operator and/or stores the information in a memory device.

SECTION 5. MODULE TESTABILITV GUIDELINES

5.0 OVERVIEW.

This section describes testability guidelines for modules, Printed Circuit boards (PCBs) and Circuit Card Assemblies (CCAs) which are independent of the circuit technology. The following guidelines are relevant to all electronic designs which are at the module/PCB/CCA level of configuration. This configuration level is sometimes referred to as a Shop Replaceable Unit (SRU) configuration level. For the remainder of this section, the term module will refer to any design at this level of configuration.

Many of the module testability recommendations and issues discussed in this section are elaborated on in other sections where specific examples of testability recommendations are provided.

5.1 Electrical Guidelines.

5.1.1 Feedback Loops.

5.1.1.1 Internal Module Feedback Loops. Internal feedback loops within a module are circuit paths with signals which propagate through one or more devices and return to the input of the source circuit. If a fault exists in this circuit then it will propagate through each device in the feedback loop and cannot be isolated. Internal module feedback loops should be designed so that the feedback path can be broken during test. This can be implemented electronically or physically.

Feedback loops can be broken electronically by using tri-state devices within the circuit or by sending the feedback signal through a controllable switch or multiplexer. More examples are given in section 7.4.4.

Feedback loops can be broken mechanically by physically disconnecting the feedback signal. The feedback signal can be broken by removing a jumper clip used to complete the signal during normal operation. In many cases the feedback jumper can be located in the backplane of the edge connector. When the module is removed for test, the feedback loop is automatically broken.

5.1.1.2 External Feedback Loops. External feedback loops are feedback circuits partially within a module that are completed by circuitry external to the module. This situation is undesirable if a complex circuit is needed to simulate the feedback input/output by the test equipment.

Complex external feedback loops should be avoided. If unavoidable, the interface portion of the feedback loop should be designed as a simple interruptible control point for the tester.

5.1.2 Sequential Devices. Sequential devices may cause testability problems because long sequences of vectors are needed to initialize or change device outputs. Sequential devices are all devices which retain a previous state (latches, charge coupled devices, and so on). Testability problems can result from the use of sequential devices if they are not properly designed to be put into known states. In the case of cascaded counters, no more than two stages should exist without test control points available which allow a tester to isolate the counters and test them individually.

5.1.3 Complex Signals. Complex signals are signals which are phase or time related that can not be monitored or supplied by standard test equipment. Tests to monitor or supply complex digital or analog signals are difficult to generate and require expensive test equipment.

5.1.4 Test Points. Test points should be located on all circuit nodes which are useful in determining the modules health. Test points should be designed so that functional circuitry cannot be damaged or degraded due to the routing or accidental shorting of a signal at a test point. Some type of test point isolation technique should be used (buffers, isolator, etc.). Test point locations are described throughout sections 7 and 12.

All test point signals must be designed with consideration that the test equipment will load the signal with additional capacitance, resistance and/or inductance. Each test point (if not on a connector) should be located to provide easy access and adequately be spaced for test clip clearance (a minimum of 5 mm clearance from anything else).

5.1.5 Redundant Circuits. Fault tolerant designs often mask errors which occur in a redundant element of the circuit. Consequently, a fault in a redundant element will not appear at the output during test. Every redundant element in a circuit should be independently testable (not effected by other redundant circuits) so that a fault can be detected at the circuit output. One way to achieve this is to make the inputs and outputs of the redundant circuits independently selectable through a MUX or by tri-stating individual redundant outputs.

5.1.6 Wired Logic. Signals which are shorted together to achieve a wired-OR or wired-AND function are undesirable since the existence of a fault is not easy to isolate. See section 12.1.2.1.2 for an example.

5.1.7 Partitioning. Every module should be designed with each major function partitioned. A module which can be divided into functional elements is easier to test than the module as a whole. See sections 7.4.5 and 12.1.3 for more information.

Every function in a module should be implemented as a complete function. Including pull-ups, bias voltages, and any other simple circuitry. Otherwise, test equipment will be required to complete the function during test.

5.1.8 Oscillators/Clocks. Every oscillator or clock which is resident on the module should be replaceable by a signal from a connector. Otherwise, ATE has to synchronize to an on-board signal, which is difficult and unreliable. Also, the test equipment may not be able to synchronize to the frequency of the oscillator. The output of an oscillator must be able to be externally disabled and replaceed by an ATE clock signal. This is true for both analog and digital circuits. See section 7.4.2 for more information and examples.

5.2 Mechanical and Physical Guidelines.

5.2.1 Repair of Components. If a module is not a "throw away" then, each component should be able to be replaced or repaired within a reasonable amount of time. The easier it is to repair a fault, the easier the design can get through the test-repair-retest cycle.

Some component assembly techniques use epoxies to mount un-packaged circuits. These designs are extremely difficult to repair. Some examples are, Chip on Board (COB) and Tape Automated Bonding (TAB). Thermally bonded devices (to improve heat dissipation) are also difficult to repair. Devices which are subject to frequent failures should be socketed.

5.2.2 Component Orientation and Marking. All components on a module should be oriented in the same direction, be identified, and have pin 1 marked. This improves component and pin location. All components (devices and connectors) should be identified by their generic part number and a component identification (ID) number (U1, P1 etc.). These markings should exist either on the component or on the module near the component, (never under the component). The markings mentioned above should be on the component side of the module and component ID numbers should appear on both sides of the module.

The component generic part numbers should also exist in the module documentation so that the component data can be gathered easily.

5.2.3 Connectors. Module connectors should be standardized to the maximum extent to reduce the need for unique factory and field test fixtures. Standard connector types and power and ground assignments should be used on as many module designs in a system as possible. In doing so, standard test fixtures can be used for multiple modules.

Connectors should be located and spaced for easy connection to ATE. Adjacent connectors should be a minimum of 250 mils apart. (See section 3.4.1).

5.3 Nodal Access.

Nodal access is necessary for ATE to have the ability to control and monitor module nodes. It is desirable to have as many control and observation points on a connector or module as possible.

Nodes must also be accessible for physical probing. Every node on a module should be able to be probed by a test program operator for fault isolation.

If a design incorporates pin-grid array.devices, then each node on the device should be physically accessible on another device or by a via or test pad.

5.4 Module ID Resistor.

Every module in a system should be designed with a unique identification (ID) resistor. The resistor should be located between two standard ID pins. This enables test equipment to verify that the proper module is mounted on ATE prior to power up during test.

5.5 Special Setup Requirements.

Designs with special setup requirements such as long warm-up times, coding, and air purity levels add restraints to ATE. Modules should be designed so that such requirements are not necessary.

5.6 Nominals.

The use of nominals and adjustments is discouraged; but if required, they must be located in an accessible location, provisions made for simple assembly/disassembly, and the number of nominals used limited to an absolute minimum.

SECTION 6. MODULE BIT/BITE

6.0 OVERVIEW.

This section describes Built-in Test (BIT) techniques that can be employed in module designs to determine if the module circuitry is functional. These BIT techniques can be used as part of a functional routine to determine module health while in an LRU or a system. They may also be employed in a module for use during module or LRU production testing.

Many of the BIT discussions and techniques described in section 4, System BIT, are also applicable to built-in test at the module level. The following paragraphs in section 4 may be applied to module level BIT.

BIT False Alarm Rate	Para.	4.8.5
System BITE		4.3
System BIT/BITE Penalties		4.1.3
System BIT Software/Hardware		4.5
ON-LINE Versus OFF-LINE BIT		4.6
System BIT/BITE Design Guidelines		4.8

All BIT techniques consist of circuitry which performs the BIT function. This circuitry is referred to as Built-in Test Equipment (BITE) and may be comprised of separate components or circuitry within functional components. The following paragraphs describe BIT techniques and the BITE circuitry used to incorporate them.

Many BIT techniques can be applied to several technologies. Rather than repeat them several times for each technology, they will only be presented once in section 6.1 - General BIT Techniques. Other BIT techniques are specific to digital or analog circuits and are described in the digital and analog sections, 6.2 and 6.3, respectively.

Several military standards apply to both system and module BIT and may also be a useful source of information. They are:

1. USAF MATE (GUIDE 3) Testability Design Guidelines (several volumes).

2. Joint Service BIT Design Guide (AFSCP 800-39).

3. MIL-STD-2165.

4. MIL-STD-2084 (BIT Requirements).

5. MIL-STD-415D paragraph 5.2.5.

6.1 General BIT Techniques.

The BIT approaches described in this section can be applied to any technology. This section also lists recommendations to improve the testability of BIT designs which are applicable to all BIT techniques.

6.1.1 Redundancy. BIT can be implemented in a design by repeating functional circuitry (creating a redundancy) which is to be tested by BIT. The redundant element and Circuit Under Test (CUT) receive the same functional input signal(s). Therefore, the circuitry of the CUT exists twice in the design and the outputs can be compared. If the output values are different and their difference is over a limit (analog circuits), then a fault exists.

This type of BIT design is expensive since an entire module function is repeated. Another expense is the additional real estate needed to implement the redundant element. Due to these expenses, redundant BIT design is usually only implemented in critical functions.

One major advantage of redundancy BIT is that it can run while the module is performing its functional operation. The additional BIT circuitry can be designed not to affect the functional circuitry in any way.

An example of a BIT design using a redundancy is shown in figure 6-1. In this example, an analog circuit is repeated and the difference between the output levels is compared. If the difference exceeds a predefined threshold, then a fault signal is generated and latched.

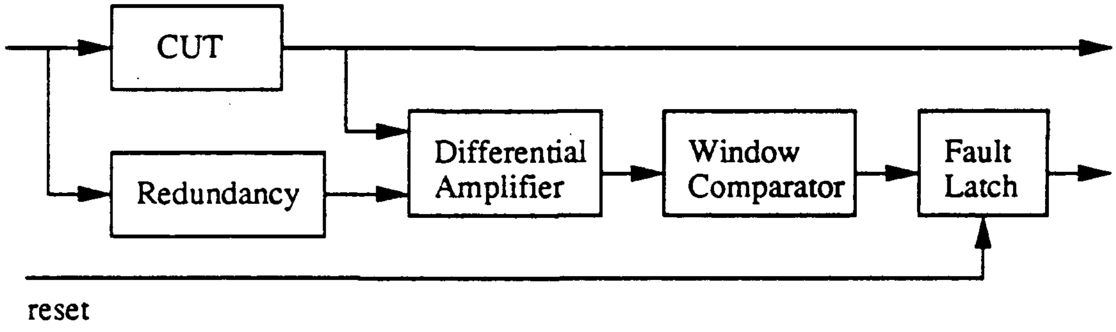


Figure 6-1. Redundancy BIT (source: RADC-TR-89-209, Vol. II)

More than one redundant element can be used. The ability to detect and isolate a fault increases as the number of redundant elements increases.

If two or more redundant elements exist, then a faulty redundant element can be isolated. The outputs signals of the CUT and each redundant element are fed into a circuit which compares these signals. This type of comparison circuit is often referred to as a voting circuit. The signal value which deviates from the others is determined to be the faulty one. The output signal values which are similar are considered correct and sent through the voting circuit. The use of one CUT and two redundant elements which feed a voting circuit is often referred to as Triple Modular Redundancy (TMR).

Whenever a voting circuit exists in a redundant design, the design must allow ATE to individually control and observe each redundant element independently. Otherwise, a fault in a redundant element will be masked by the voting circuit from appearing at the voting circuit output.

6.1.2 Wrap-around BIT. Wrap-around BIT requires and tests microprocessors and their input and output devices. During test, data leaving output devices is routed to input devices of the module. The BIT routine is stored in on-board ROM. Wrap-around can be done by directing output signals from the processor back to the input signals and verifying the input signal values.

Wrap-around BIT can be applied to both digital and analog signals concurrently. An example of wrap-around BIT testing both analog and digital devices is shown in figure 6-2. In this example, during normal operation processor outputs are converted from digital to analog outputs and analog inputs are converted to digital input signals. When the BIT is initiated, the analog outputs are connected to the analog inputs and the signals are verified by the processor.

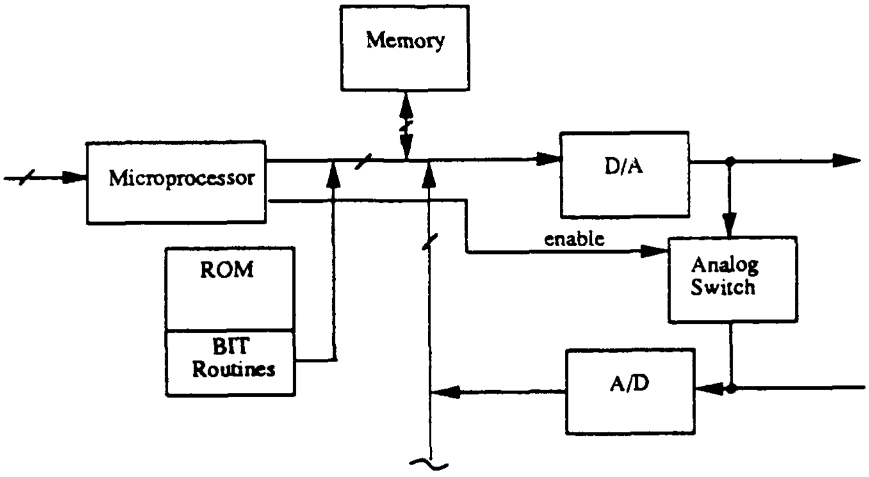


Figure 6-2. Wraparound BIT (source: RADC-TR-89-209, Vol. II)

6.1.3 Generic BIT Testability Rules. The following is a list of testability rules which are applicable to all forms of BIT design and technology. Following these rules allows easy access to observe and control BIT routines as well as isolate BIT detected faults.

1. Provide access to all BIT control and status signals at module connector pins. This will enable ATE to directly connect to BIT circuitry.

2. Incorporate complete BIT functions and BITE on the module. If only a portion of the BIT routine or BITE circuitry exists on the module then ATE cannot utilize the BIT routine without providing the missing BIT functions.

3. If possible, design BIT as "fail-safe" BIT. Fail-safe BIT will contain a BIT fault so that it will not disrupt functional circuitry.

4. Devices used as BITE should have a higher reliability then the function being tested. If the failure rate of the BIT circuitry exceeds that of the function being tested, then the probability of a failure or the inability to report a failure will most likely be due to the BIT circuitry. This contradicts the purpose of incorporating BIT.

5. Critical voltages should be visually monitored by sending the voltage signals to visible LEDs.

6. BIT failures should be latched on the module. This makes it easier for the system or ATE to poll the error bit at any time.

7. BIT test times should be kept to a reasonable limit. Many BIT routines use pseudo-random number inputs which often take a long time to generate high fault coverage. BIT routines in modules should be limited to under ten (10) minutes.

8. If many BIT routines exist on a module then ATE should have access and the ability to control each routine individually.

9. BIT routines are usually controlled by a processor. If this processor exists on the module, then the BIT routines can be externally controlled by ATE. If the processor does not reside on the module, then the ATE must provide the instructions that the BIT processor provides in the system during test.

6.2 Digital BIT.

There are many ways to implement BIT in digital circuits. The major ones will be discussed herein. General digital BIT testability guidelines will also be provided.

6.2.1 On-Board Integration of VLSI Chip BIT. Some VLSI devices on a module may already incorporate a Built-in Self Test (BIST) routine. The processor used to control module BIT initiates BIST of chips. After the VLSI tests are complete the processor can poll the VLSI status signals to verify the BIST routines passed.

If a processor controls individual VLSI BIST routines, then ATE should be able to individually control VLSI BIST routines either through the processor or by VLSI control signals.

6.2.2 Signature Analysis. Signature analysis is often used as an adjunct to several testing methods including incircuit and functional and serves basically as a data compression technique.

To perform signature analysis, data is applied to a Circuit Under Test (CUT) and the circuit outputs are compressed into a signature and compared against a known correct value.

Figure 6-3 shows an example of a circuit which uses signature analysis to perform BIT. During test mode, the inputs to the CUT are switched from module inputs to programmed inputs from the device marked PRG. These signals must always repeat a sequence of values every time the test is initiated.

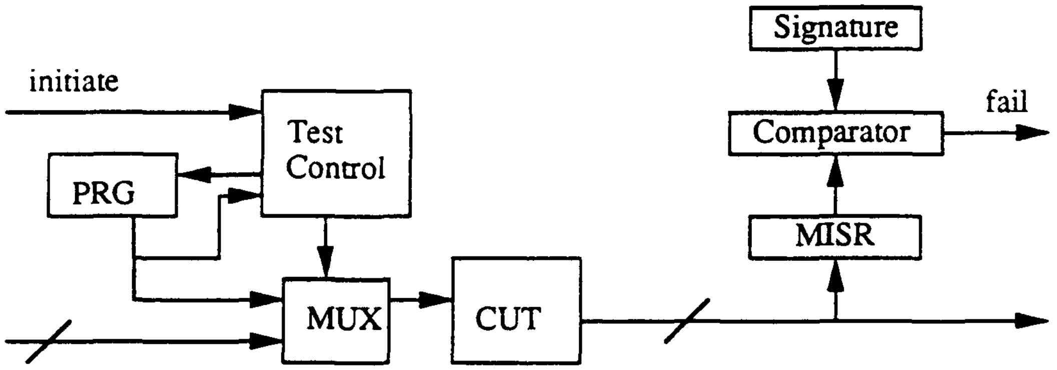


Figure 6-3. Signature Analysis (source: RADC-TR-89-209, Vol. II)

Data compression is achieved in the signature analyzer by accepting data from the CUT for each and every circuit clock cycle that occurs within a circuit-controlled time window. Within the signature analyzer is a multiple input shift register (MISR) into which the data is entered in either its true or complement logic state, according to previous data-dependent register feedback conditions. This signature is then a characteristic number representing time dependent logic activity during a specified measurement interval for a particular circuit node. Any change in the behavior of this node will produce a different signature, indicating a possible circuit malfunction. A single logic state change on a node is all that is required to produce a meaningful signature.

Serial data is shifted into the register along with a start, stop, and clock signal. The remainder uniquely defines nodal states and times as long as enough patterns have been circulated through the shift register. Input stimulus vectors can either be provided by onboard software or from an external source such as an ATE system or in-circuit emulator.

Signature analysis often u<es pseudo-random inputs. The effectiveness of signature analysis with pseudo-random inputs is decreased as the number of sequential devices and high input AND-gate devices increases. This is because specific inputs or sequences of inputs need to be applied to sequential and high input AND-gate devices.

6.2.3 Built-in Logic Block Observation (BILBO). This BIT technique takes the scan path and Level Sensitive Scan Design (LSSD) concept and integrates it with the signature analysis concept. See section 11 for a discussion of the LSSD and scan concepts. The end result is a technique for BIL3O.

BILBO BIT design uses elements referred to as BILBO registers (or BILBO latches). A BILBO register is a circuit which can act as a latch, linear shift register, multi-input shift register, pseudo-random number generator, or a reset register.

BILBO registers act as normal registers during normal operation. They can be controlled to enter another mode via input control signals.

An example of a design incorporating BILBO registers is shown in figure 6-4. In this circuit two BILBO registers are placed at the inputs and outputs of combinational circuitry. During normal operation these registers act as latches. They can be externally controlled to enter a different mode of operation and loaded with serial data to initialize the shift register contents.

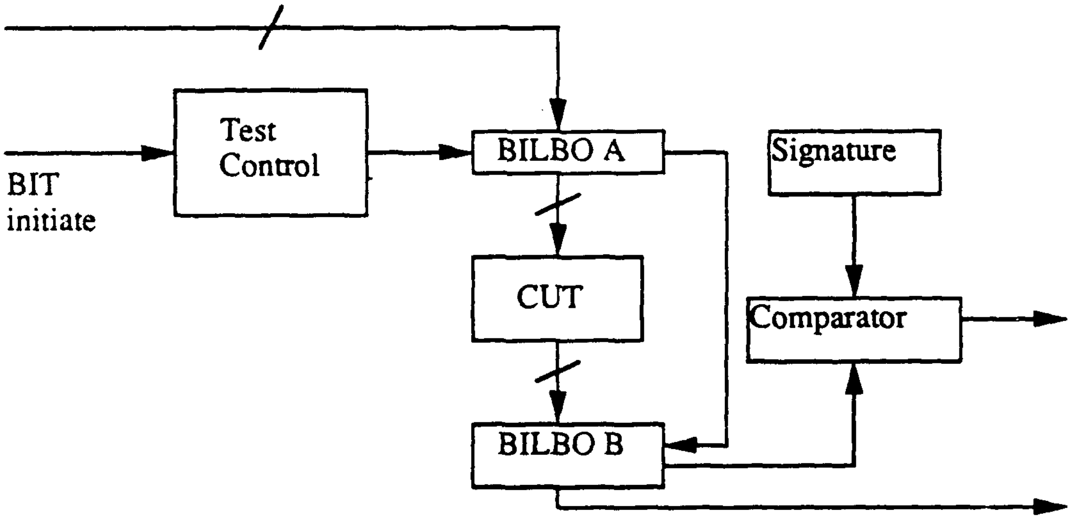


Figure 6-4. Built-in Logic Block Observer (BILBO)

To run BIT in the design shown in figure 6-4, the BILBO registers are first put into the proper modes and initialized. BILBO A is put into the pseudo-random number generator mode and initialized with a seed value. It will output a sequence of number patterns that are very close to random patterns. Repeatable random patterns can be generated quite readily from this register. These sequences are called pseudo-random number (PN) patterns. BILBO B is put into a Multiple Input Shift Register (MISR) mode and also serially initialized to a seed value. The MISR BILBO device acts as a data compressor and can generate a signature.

The BILBO A register is used as the PN generator. The output of the BILBO A register will be random patterns. This will perform a reasonable test of the combinational logic, if sufficient numbers of patterns are applied. The results of this test are be stored as a signature in the BILBO B register. After a fixed number of patterns have been applied, the signature is scanned out of the BILBO B register for comparison against a known correct signature.

This technique solves the problem of test generation and fault simulation of combinational networks that are susceptible to random patterns. There are some known networks that are not susceptible to random patterns. They are programmable logic arrays (PLAs). The reason for this is that the fan-in in PLAs is too large to effectively use random inputs. Random combinational logic networks with a maximum fan-in of 4 can be efficiently tested using random patterns.

6.2.4 Coding Schemes. Data can be coded such that a simple analysis of the coded data can determine if an error in one of the coded data bits has occurred. Using coding schemes is an effective way to perform BIST on data transmission and storage. They require that several additional bits of data are added to the un-coded data. The coding scheme is applied to the data prior to transmission or storage and is verified when the data is received or retrieved from memory.

Coding schemes can be applied to data which is stored on the module. When the data is retrieved, the coding scheme can be reapplied to verify that storage or transmission faults have not occurred. If the coding scheme alters or re-codes the un-coded data , then the data is un-coded prior to transmission when it is retrieved from memory.

6.2.4.1 Parity Check. a very simple implementation of a coding scheme is to add an extra bit to several bits of data for parity. This parity bit is set to a value which when added to the data bit adds up to an even or odd number. The parity bit is set for every data word which is transmitted or stored and transmitted or stored with the data bits.

Two types of parity are possible. If the sum of the data bits and parity is even, then the coding is called 'even parity'. If the sum adds up to an odd number then the coding is called 'odd parity'.

6.2.4.2 Hamming Code. A hamming code actually alters the data bits into a coded word with more bits than the un-coded word. If enough additional bits are added to the un-coded word, then the hamming code can detect, isolate, and fix a faulty bit.

6.3 Analog BIT Techniques.

Analog designs often have more BIT per functional unit than digital designs. Analog BIT usually takes the form of sensors or transducers (such as, diodes, thermo couplers, encoders, and synchros) which monitor a condition. The monitoring outputs are then sent via an Analog to Digital Converter (ADC) to digital circuits for a further analysis or digital output.

Many digital BIT techniques can be applied to analog designs after the analog signals are converted to digital signals.

Analog BIT is difficult to develop because analog devices have many failure modes. Unlike digital, analog circuits often have tolerance faults. These faults can be detected by BIT but acceptable thresholds have to be determined and incorporated into the BITE design.

High frequency signals are subject to noise interference and can be disrupted by BITE. Care should be taken to monitor such signals without disrupting the functional operation.

6.3.1 Voltage Summing. Analog voltage levels can be confirmed by summing them and comparing the sum against a threshold. A circuit which incorporates voltage summing BIT is shown in figure 6-5. This type of design is good for power supply monitoring. However, it is only useful on static signals.

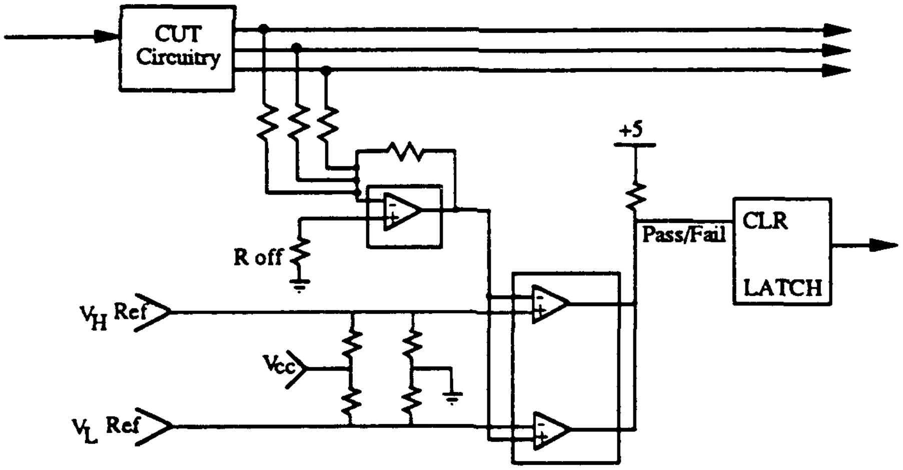


Figure 6-5. Voltage Summing BIT (source: RADC-TR-89-209, Vol. II)

6.3.2 Comparator. This type of BIT is similar to signature analysis for digital designs. A known value is input to the Circuit Under Test (CUT) and the output is compared against a correct known value or function. An example of a comparator BIT circuit is shown in figure 6-6.

In this example, multiplexors (with select inputs labelled G) are used to replace the CUT input with a test signal and directs its output to a signal processor. This type of design ᶜᵃn be applied to many types of analog circuits. The output of the CUT is processed and compared to an expected value. The test signal and expected outputs can be static signals or waveforms.

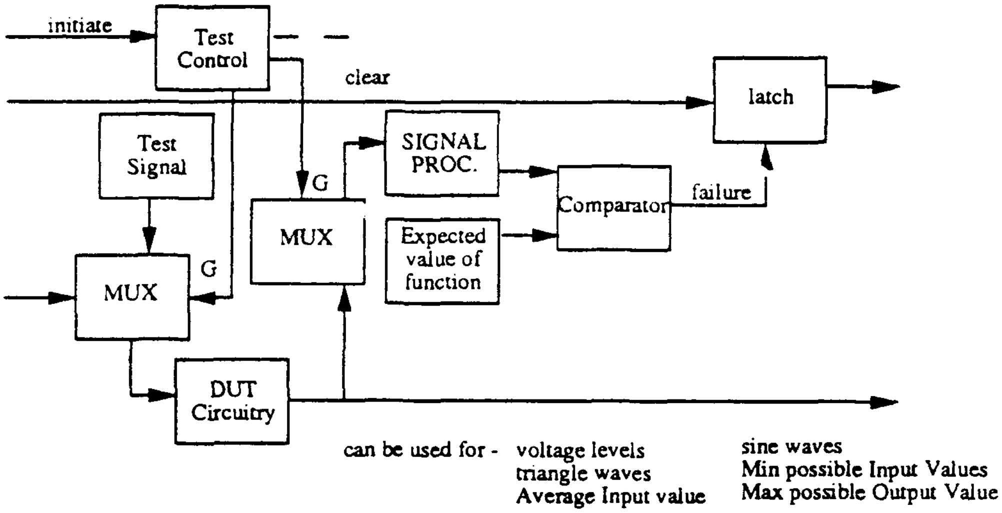


Figure 6-6. Comparator BIT (source: RADC-TR-89-209, Vol. II)

6.3.3 Analog BIT Testability Rules.

1. High frequency signals which are tested by BIT must not be disrupted to the point of disturbing the functional operation. Directional couplers can be used to monitor such signals without disturbing them.

6.4 BIT Evaluation.

There are several ways to evaluate the effectiveness of a BIT design. Some are as follows:

1. BIT Evaluation Parameter Analysis
2. Failure Modes and Effects Analysis (FMEA)
3. Fault Simulation
4. Statistical Analysis

6.4.1 BIT Evaluation Parameter Analysis. The following is a list of parameters that can be evaluated to determine the effectiveness of a BIT design. Some of these parameters are discussed in section 4.

1. Mean fault detection time
2. Frequency of BIT executions
3. Fault isolation resolution
4. Test thoroughness
5. Fraction of faults isolated
6. Mean fault isolation time
7. Maintenance personnel skill level
8. BIT reliability
9. BIT maintainability
10. BIT availability
11. Mean BIT running time

The relative importance of each parameter should be agreed on by the manufacturer and contractor prior to determining these parameters.

6.4.2 Failure Mode and Effect Analysis (FMEA). To implement this technique which is based on existing failure probabilities, the following steps are needed:

1. Ensure known major failure modes have been evaluated and are detectable and isolateable by BIT.
2. Provide estimate of BIT fault detection and isolation.
3. Make 2nd level BIT hardware design.
4. Make guidelines for BIT software development.
5. Define LRU interfacing requirements to facilitate BIT.

% faults detectable = ffr/sfr x 100 $\quad$ ffr = Σ fault failure rates detected by BIT

% isolateable = ifr/sfr x 100 $\quad$ ifr = Σ fault failure rates isolated by BIT

sfr = Σ all failure rates

6.4.3 Fault Simulation. Fault simulation of module/LRU is usually quite expensive and models take a long time to develop for individual LRUs and faults.

Faults are placed in the simulated design and simulated to determine if the BIT design can detect them. Every possible fault needs to be analyzed in this manor to fully test the BIT design.

A quicker method is to take a sample of the most important/critical faults and estimate total BIT coverage. However, this method is less accurate..

6.4.4 Statistical Analysis of BIT. When applying a statistical analysis of BIT several questions have to be asked first:

1. What is the probability of BIT generating false alarm?
2. What is the probability of BIT missing a fault?
3. What time is needed between BIT checks?

Once these questions have been answered, a statistical common analysis is performed to verify BIT effectiveness.

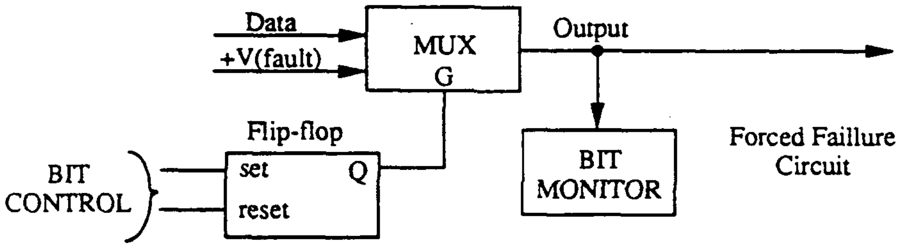
6.5 <u>BIT Verification</u>.

BIT can be designed so that it can also test itself with Built-in Self Test (BIST) routines. This is an important feature because when BIT circuitry is added to a design, the circuitry (BITE) is part of the design. It must conform to the same fault detection and failure rate requirements that the rest of the design conforms to.

BITE verification tests or self tests should always be performed prior to the main BIT routines. If the BITE verification tests fail, then a failure in the BIT circuitry should be reported. Any other tests which use the faulty BITE should then be disregarded.

6.5.1 <u>Self Checking BIT</u>. The BIT circuitry is designed so that a fault in the BIT circuitry will cause the BIT circuitry to output a fault status signal.

6.5.2 <u>Fault Insertion</u>. During BIT self test a fault is directed to the input of the BIT design. If a fault status signal is not generated by the BITE, then the BITE is faulty and a fault signal is output. An example of fault insertion BIT is shown in figure 6-7 (G represents the MUX select lines).



NOTE: It is difficult to represent entire fault population. Thus, this technique may not be very thorough.

Figure 6-7. Fault Insertion BIT (source: RADC-TR-89-209, Vol. II)

It is difficult to represent a large portion of failure modes with this type of self test.

6.5.3 Overlapping BIT. The module or UUT is partitioned into segments. Each possible fault within a segment is tested by two overlapping BIT routines. An example is shown in figure 6-8. Since any fault is tested by two BIT routines, if only one BIT routine reports a fault, then a fault must exist in a BIT routine or the BITE that the routine uses.

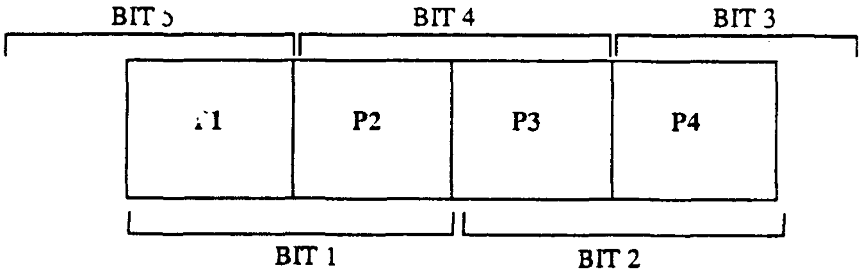


Figure 6-8. Overlapping BIT (source: RADC-TR-89-209, Vol. II)

SECTION 7. DIGITAl GUIDELINES

7.0 OVERVIEW.

Testability considerations should arise during the initial design stages. The ease with which a board can be tested and fault isolated should be one of the design engineer's major concerns. Employing a few basic guidelines during the design phase can result in far reaching rewards during the design of the assembly.

The purpose of sections 7 through 11 is to discuss digital testability guidelines and demonstrate how to improve the testability of digital hardware. Section 7 concentrates on digital designs which use small or medium-scale integrated circuits (SSI and MSI) on a module or CCA. Sections 8-11 address the design for testability of digital circuits using Large Scale Integration (LSI) or Very Large Scale Integration (VLSI) circuits.

A testable design will allow the verification of correct operation and fault isolation of the circuit to some hardware level. The level of fault isolation is established by specification, and may be the replaceable part (module or assembly), the circuit component, or logic internal to the circuit component depending on the point in the life cycle at which the test is being performed. It is the responsibility of the design engineer to determine the test requirements for his design and to implement the design in such a way that those requirements are satisfied.

The design requirements for test are determined by criteria which define: (1) when the test is acceptable (for example, "should detect 98% of all single occurrence of stuck-at faults within 3.2 seconds."). and (2) what the fault ambiguity level must be. The ambiguity group on a CCA should be three devices or less, as detected from the edge or from a test-only connector.

With the requirement established, the designer can produce a testable design which is compliant by incorporating the following three features:

- Initialization -- The internal status of the circuit can be set or programmed to a known initial state.
- Visibility -- The state of any element of the circuit can be directly determined.
- Controllability -- The state of any circuit element can be changed in a known fashion.

These elements are discussed in greater detail in sections 7-1 through 7-4.

7.1 Initialization.

Initialization means "setting a starting position, state, or value". In testing digital storage elements, this refers to the ability to control the initial state of registers and sequential circuits. The initial state of a circuit describes the contents of the storage elements, immediately after applying power.

Many designs do not need a specific initial state to function correctly. A circuit may continue along a specific sequence from an arbitrary start point or the system that the circuit is embedded in may alter the circuit inputs to eventually achieve a predictable condition. However, for test or simulation purposes, the circuit storage elements must be in a known state. This can be achieved by employing an initialization sequence to the UUT before testing. Such an initialization sequence may be very long causing increased software expenses, additional test time, and time-consuming troubleshooting procedures. These problems can be avoided by incorporating adequate initialization ınto the design.

7.1.1 Initialization Techniques. The two basic methods for initializing a circuit are, (1) external control, and (2) self-initialization.

1. External control methods may only use unused edge connector pins, while others require the addition of logic elements whose only functions are to enhance testability.

2. Self-initialization can be implemented through a simple RC power-up reset or through a short clock sequence that converges on a known circuit state. As a rule of thumb, less than 64 clock pulses should be applied to a UUT to achieve initialization. Any longer than this increases the probability that circuit faults will cause the UUT to fail unpredictably when it does not initialize correctly. Any ATE diagnostic technique, such as guided probe or fault dictionary, will be virtually useless in these cases as faults often cause erratic, unpredictable outputs.

In general, external initialization control is preferred over self-initialization to the extent that an external override or inhibit may be added to a self-initiating circuit. This may avoid powering down a UUT just to use a power-up reset or inhibit a self-resetting circuit for test purposes.

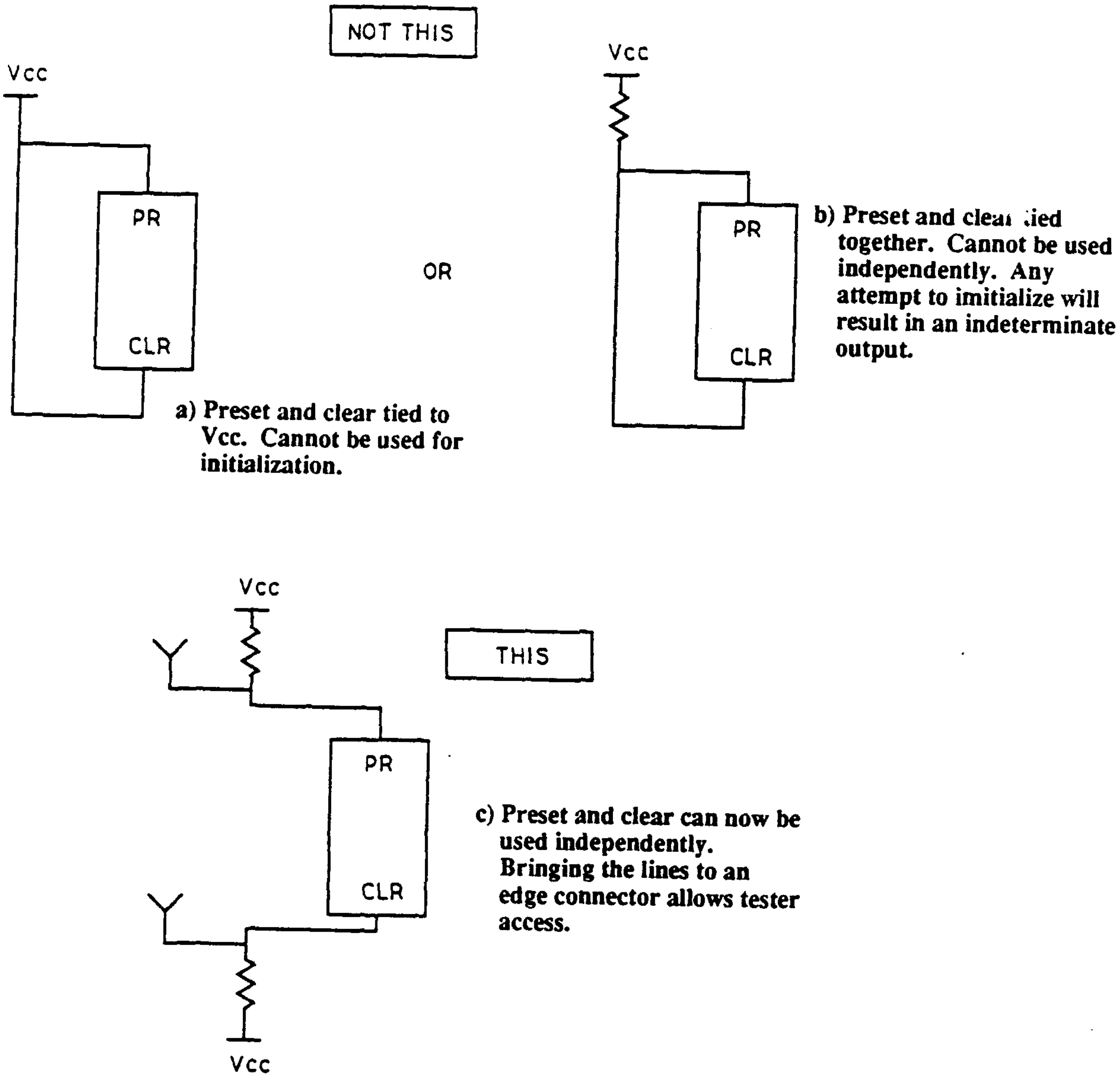
The following sections give some practical explanation on initialization techniques.

7.1.2 Basic Initialization Guidelines.

Shown in Figure 7-1 are two common circuit configurations , (a) and (b), that illustrates a frequently missed opportunity to improve initialization of the basic storage element, the flip-flop.

In configuration (a), the preset and clear are unusable as they are tied directly to the power bus. Configuration (b) is no better as ꞔonnect both signals to the same pull-up creates a race condition.resulting in an unknown state.

Configuration (c) demonstrates the ideal case where preset and clear are independently controlled via an external connection. This external connection may to an edge connector pin (preferred) or to a special purpose test connector. (Do not depend on an IC clip/flying lead access as the UUT may be conformably coated!).



a) Preset and clear tied to Vcc. Cannot be used for initialization.

b) Preset and clear tied together. Cannot be used independently. Any attempt to imitialize will result in an indeterminate output.

c) Preset and clear can now be used independently. Bringing the lines to an edge connector allows tester access.

Figure 7-1. Device Initialization Example

When multiple storage elements are present on a CCA, the number of control points and components for testability can be reduced as shown in the three examples provided in Figure 7-2. Her again, edge connector access is best.(a). A power-up reset can also help from the standpoint of go-no-go testing, but provides little help in the area of fault diagnosis if the power-up reset circuit faults (b). If a logic "0" is required, an inverted with its input tied high (c) may be used.

The inverter input can be brought to an edge connector, or, if that is not possible, can be accessed by a "test only" connector to override the logic state. Connecting an unneeded (from a functional stand point) initialization point directly to voltage or ground bus points should be avoided.

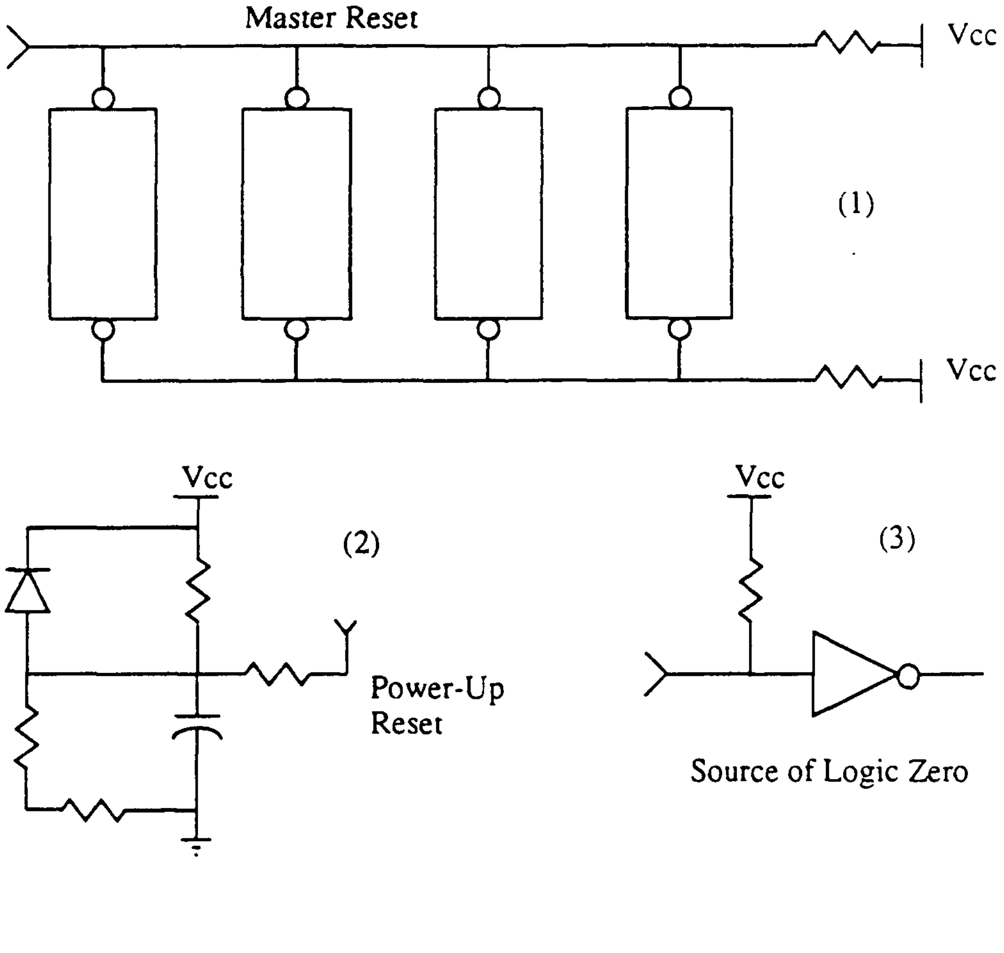
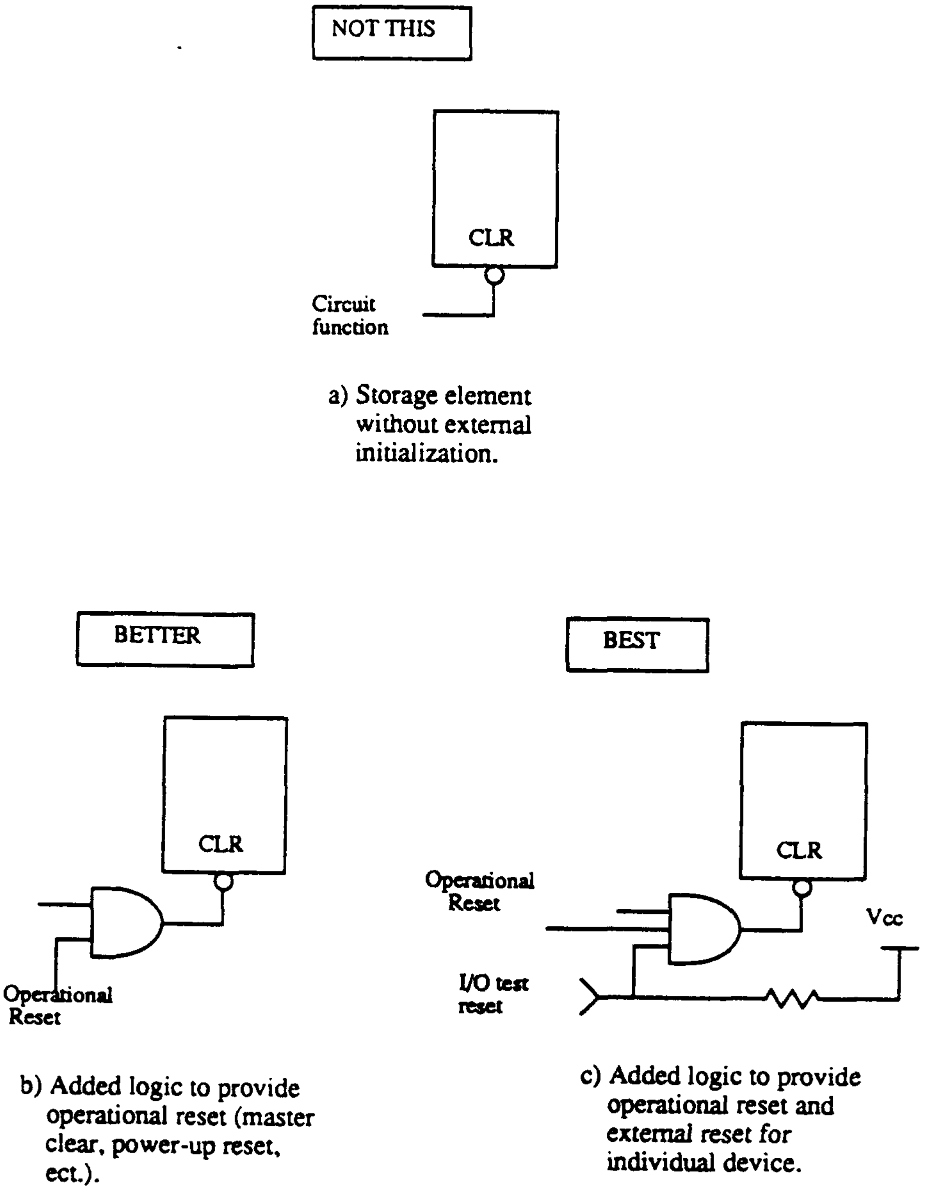


Figure 7-2. Initialization of Multiple Storage Elements

In certain cases, it may be necessary to add a logic element to a CCA to allow for proper initialization. Bringing the control of this extra logic element to the edge connector or to a "test only" connector facilitates the production test process (see example (c) in Fig. 7-3).



a) Storage element without external initialization.

b) Added logic to provide operational reset (master clear, power-up reset, ect.).

c) Added logic to provide operational reset and external reset for individual device.

Figure 7-3. Recommended Control of Device Initialization

7.1.3 Initialization Examples. The example provided in Figure 7-4 shows a frequently used divide-by-four counter which generates internal clock pulses and runs continuously as long as the inhibit line remains LOW. However, when the inhibit line goes HIGH, the counter continuous to run until it reaches a count zero state; thus, it is self initiating.

Two factors limit this type of circuit suitability for automatic testing. First the circuit requires one to three clock pulses for logic initialization at "power on". As the number of divide-by-two networks increases, the number of required initialization clocks increases exponentially. Second, the circuit may never be initialized if a fault occurs during the initialization procedure. In such a feedback network, these faults are difficult to find because they are often not repeatable. By designing the circuit shown in the above example of Figure 7-4, automatic testing can be achieved. In the ATE design, the reset line can remain unconnected in the back-panel wiring, but should be tied to the appropriate voltage via a resister on the CCA.

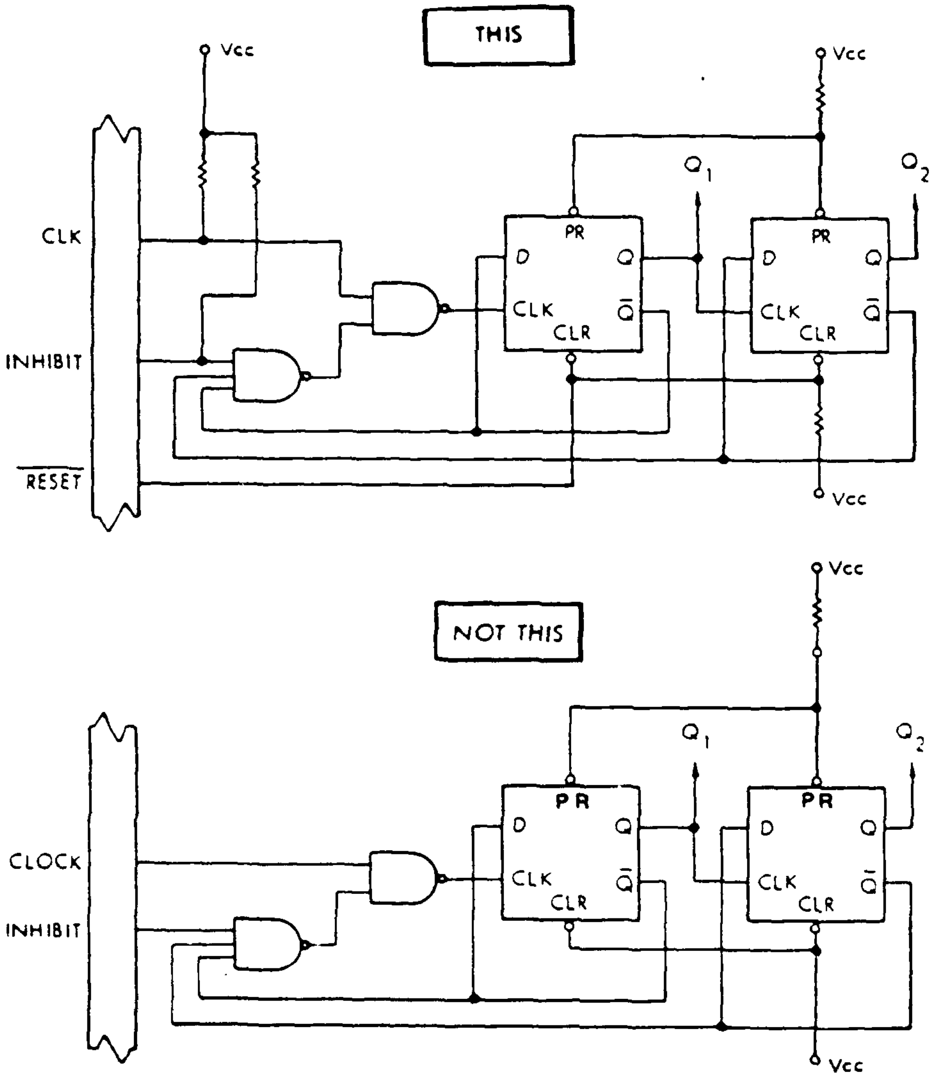


Figure 7-4. Initialization Circuit Example

7.2 Visibility.

The ability of the external system to observe or view the function or non-function of module internal circuits is the module's visibility. The visibility requirement is to incorporate test points, data paths, and circuitry to provide the test system sufficient data for failure detection and isolation within the module. The selection of physical (real) test points should be suffi~~ent to accurately infer the value of internal nodes (virtual test points) of interest. There should be no requirements to probe internal points for organizational level fault fault isolation. As a rule of thumb, the UUT active nodes should be available to the tester through I/O or test connectors. Visibility reduces the complexity of the test interfaces and therefore reduces the cost of test program set acquisition, and skill levels and man-hour expenditures in operation and maintenance.

7.2.1 Implementation. The following techniques may be used to build visibility into the system/module.

1. Use spare I/O pins to provide access to internal nodes otherwise unavailabi. (but do not leave floating when used in the system). These internal nodes can aid in testing glue logic (Small Scale Integration) or more complex devices.

2. Select test locations for maximum access (and control) to buried nodes. strategic placement of test points is far more important than quantity. Critical locations for test points are:

    - In feedback loops to break/control important signals.
    - To subdivide counter chains and long sequential logic paths.
    - At wired AND connections (if unavoidable) and similar high ambiguity paths.
    - At points where high fan-out or high fan-in exists (Fig, 7-5).
    - On any bus enable signal paths.
    - On ~used logic lines.
    - On memory enable lines.
    - On chip disable bus lines.
    - On ROM data lines, especially if remaining logic is controlled by ROM contents.
    - Between logic blocks.
    - In circuits with redundant (fault tolerant) logic.
    - On interfaces between analog and digital circuitry.

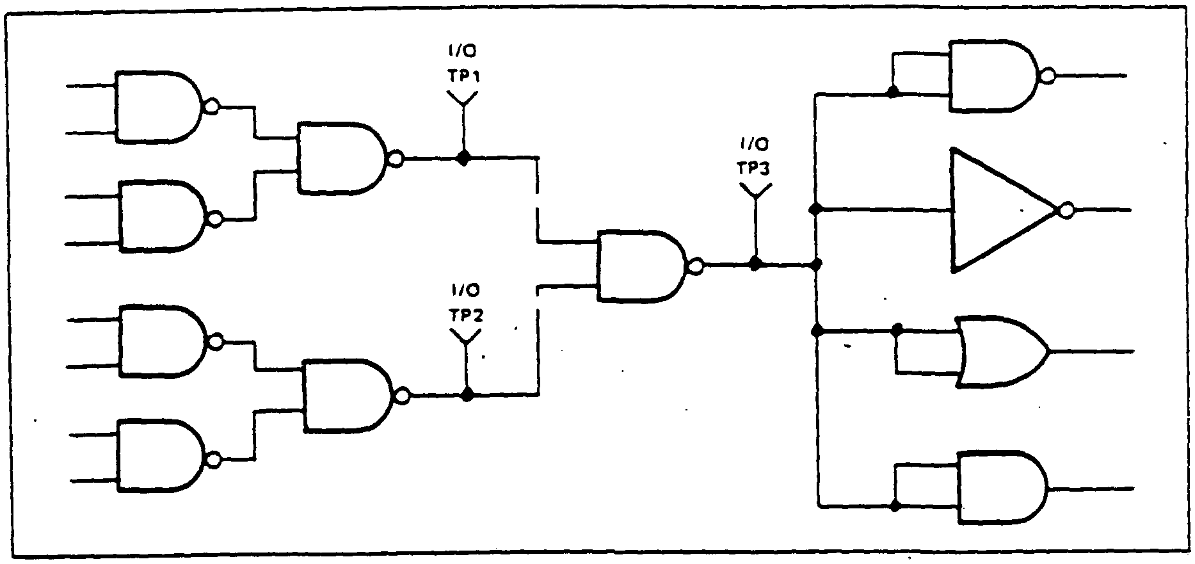


Figure 7-5. High Fan-Out/High Fan-In Test Point Placement

3. Use display Lighting Emitting Diodes (LEDs) on the Printed Circuit Boards (PCBs) to indicate proper operation of important circuits, Examples are: power supply voltage is on, clock is present, or phase-lock-loop is locked.

4. Use positive indication fault indicators and displays so that a good test always results in an ON condition. A defective indicator or display then always indicates a fault condition, either attributable to the input or its being faulty.

5. For a critical display, use an alternate method of testing, such as push-to-test, to provide positive verification of its operation.

6. As a rule of thumb, do not exceed four stages of sequential logic "depth" before providing a test point.

7. In the example shown in Figure 7-6, multiple LED testing requires the operator to visual observe each LED as the PCB is tested. To reduce test operations, advantage can be taken of ATE by measuring logic level at the LED test point and then performing one operator visual test with all LEDs lit.

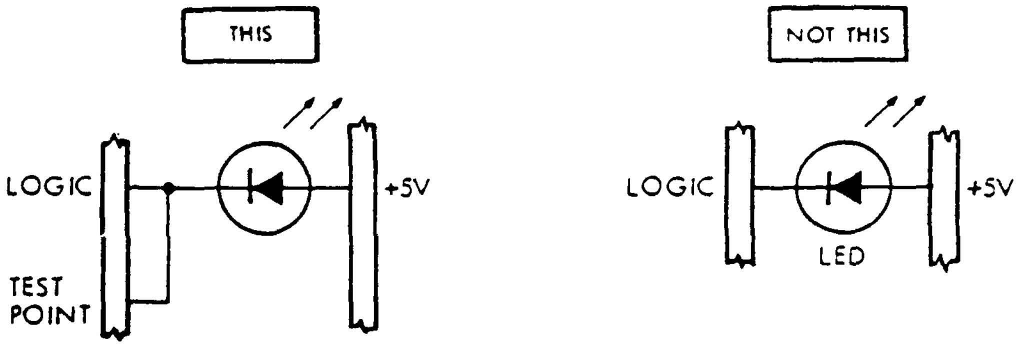


Figure 7-6. ATE Test Operation Improvement

8. Multiple inverters in a common package need only one observation point when connected as in Figure 7-7. The dotted lines are not necessary because they all come from U1. If any output from U1 is faulty, such as, U1D in this example, U1 should be replaced. This can be determined from the U1D output visibility test point.

   A similar situation exists in delay lines where each output has an additior.-¹ delay from the input. The delay of the last delay output can be measured and indirectly verify all of the preceding delay lines.

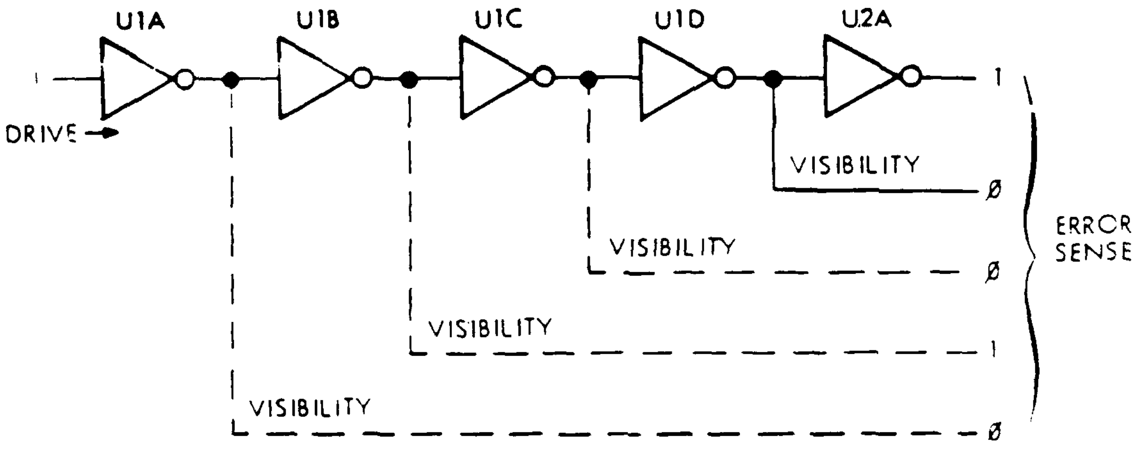


Figure 7-7. Reduction in Visibility Points

9. Visibility may also be improved by accessing test points in a multiplexed or serial manner rather than by dedicated parallel pins. A scan-path or boundary scan architecture can improve testability without the need for many additional test points (see section 11).

7.3 Controllability.

It is desirable to have the ability to change the state of any internal storage element directly. While the design of the logic assemblies does not always lend itself conveniently to this feature, the designer should attempt to provide as much capability in this regard as possible.

The following features (covered in detail in section 7.4) will result in enhanced testability when incorporated:

- Clock/Set/Reset control for storage elements e.g. counters, flip-flops, etc.
- Feedback loop control.
- Read/Write/Enable control for memory devices.
- Hold/Reset/Enable control for microprocessors.
- Control of tri-state device output and enable lines.
- Data/Address/Enable control on any bus-structured design.
- Select control for multiplexer/demultiplexer devices.
- Inhibit and/or override of on-board oscillators/clock generators.
- Partitioning of large complex circuits to reduce the test generation task.
- Internal pattern generators for special tests. Control of asynchronous circuits (e.g. monostables, self-resetting etc.).
- Use serial/scan or multiplexing to increase control of internal nodes when extended I/O is restricted.

Each design is unique, and the problem of controllability is one which must be addressed in terms of the design requirements. The tradeoff which produces the test implementation must be a part of the design review documentation.

7.4 Functional Elements.

7.4.1 Introduction. This section includes specific examples of functional circuits and the recommended approach which will ensure testability. The demonstrated techniques are not presumed to be exhaustive, but are presented as typical of the recommended treatment of commonly used functions.

In general, each circuit requires some added hardware to allow or to facilitate testing. This hardware is designated "BITE", or Built-In Test Equipment, and involves any circuitry which has no functional use but has been added to allow testing of the circuit, including control functions, monitor points, lights, switches, buffers or any other circuitry of this type.

The designer must also consider reliability and cost (life cycle cost, not just design cost) when adding BITE. Considerations include the amount and complexity of the added hardware and the possible software/firmware cost impact versus the savings over the life of the equipment which the BITE will produce.

7.4.2 Oscillators/Clocks. The most serious testability problem in logic design is a free-running oscillator buried within the logic - one which is not accessible from an edge connector and therefore not controllable by the testing device. The tester must then establish its own time reference and maintain synchronism, which is not easily achievable and leads to many problems in repeatability and diagnostics.

Another test problem occurs when the internal clock speed of the circuit is faster than that of the tester (>10 MHz). In this case the UUT logic can sequence Through several states during one tester clock cycle, making it impossible for each UUT state to be verified on an independent basis.

To improve the testability of one UUT, it is necessary to to replace the buried oscillator with an externally generated clock. This allows the tester to run at a slower speed and to properly synchronize with the UUT. Additionally, this can also help in the debug phase of test generation, especially if the UUT can be single-stepped. Some method of controlling buried oscillator are shown in Figure 7-8.

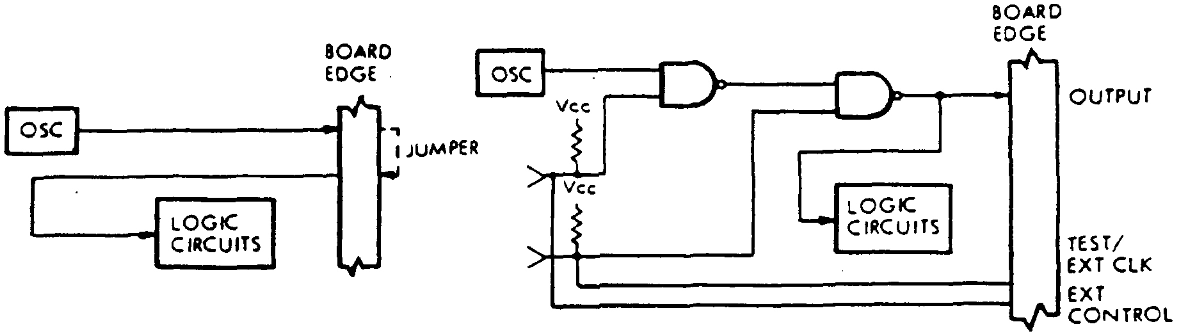


Figure 7-8. Methods of Freeing a Buried Oscillator

1. Isolation of an Oscillator - Partition the circuit so that the output is brought to the module connector. Then provide an external oscillator input to the logic circuitry that can be jumped at the board edge for normal operation or used as a direct input from the tester. Locate the oscillator circuit near the module connector to allow short runs and minimize signal pick-up or cross-talk. (This may not be desirable for very fast clock circuitry).

2. External Control of an Oscillator - Provide a method to disable the UUT oscillator and allow an external tester clock to be applied. In normal operation the test/external clock and external inputs are open (but terminated via resistor network). Under test, the tester drives the external control input LOW while providing its own clock to the test/external clock input.

7.4.3 Interface. The designer must consider two classes of interfaces: The interface to the UUT which is necessary for stand alone test using ATE, and the in-place (system or subsystem) interface, such as the bus. Each of these interfaces presents a different type of problem. The ATE interface may require a special level conversion to assure compatibil'ty, while internal interfaces will require special treatment and should be considered on a case-by-case basis.

7.4.3.1 Special or Mixed Logic Levels. Circuits designed with logic levels other than Transistor-Transistor Logic (TTL) levels require special considerations. Most test equipment is TTL compatible, and level shifters, buffers and other circuitry must be added to test adapters when testing other types of logic. To lower these interface costs. all I/O should be made TTL compatible if possible and practical. If mixed logic levels must be used, the non-TTL level should be sandwiched between TTL levels so that the TTL logic is at the board edges, as shown in Figure 7-9. The board should not be overpopulated in order to provide .his feature (e.g., circuitry that exceeds fivε percent of the functional density is too much).

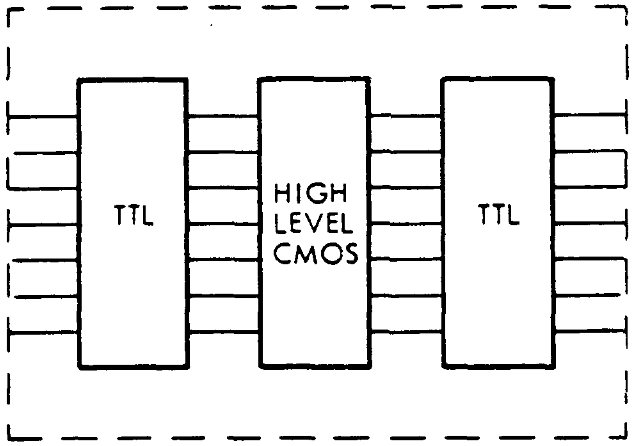


Figure 7-9. Interfacing of Mixed Logic Levels

Life cycle costs must be considered here. For example, when a large production run is projected, the adapter for non-TTL levels could be built into the factory test equipment. If field test equipment will have no test adapters, then this approach may not be cost effective over the life of the equipment, even though it appears to be best during production.

7.4.3.2 Edge-Sensitive Components. Edge sensitive components should always be buffered (or latched) from primary and test I/O. The purpose of buffers is to prevent noise (input) or overloading/transmission line reflections (output) from entering a circuit where a memory element can be arbitrarily set or reset. The example presented in Figure 7 - 10 demonstrates the inclusion of a buffer that eliminates a potential testability problem caused by excessive ATE or system noise. Storage elements should always be buffered prior to the module connector. Clock inputs should always be reshaped (clean up the edges by buffering) on the module prior to functional usage.

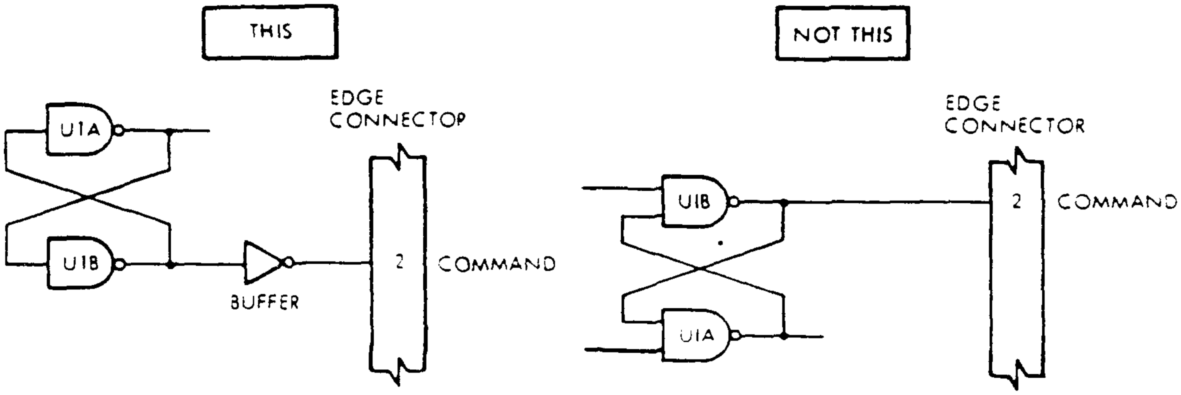


Figure 7-10. Use of Buffers

7.4.3.3 Bused Logic. Systems designed with interconnecting buses do not present major circuit board testing problems unless the bus is contained entirely on the board. It then becomes a problem similar to testing fan-in and fan-out logic implementations, except that the devices which access the bus are, in general, tri-state. Tri-state "enables" for these devices must be made controllable by ATE, and all buses must be accessible from the edge connector pins or a "test only" connector. The best approach is to allow ATE to control individual devices which access the bus. Individual control improves the possibility that the ATE can diagnose a failure to a single device. If this is not possible, then groups can be controlled to isolate the fault to subsections of the bused logic.

A special case of bused logic exists when the logic on the boards is controlled by the contents of a ROM. In this situation the designer must insure that the tester will be able to control the bus. Figure 7-11 illustrates how the ATE maintains access to the address lines, tri-state control, and the bus. The ATE can read the contents of the ROM, disable the ROM outputs, and then drive the bus with its own test pattern - all through the I/O connector.

(Note: Figure 7-11 can be applied to any bus configuratio⁻ ᵗo illustrate how an internal bus can be made externally accessible).

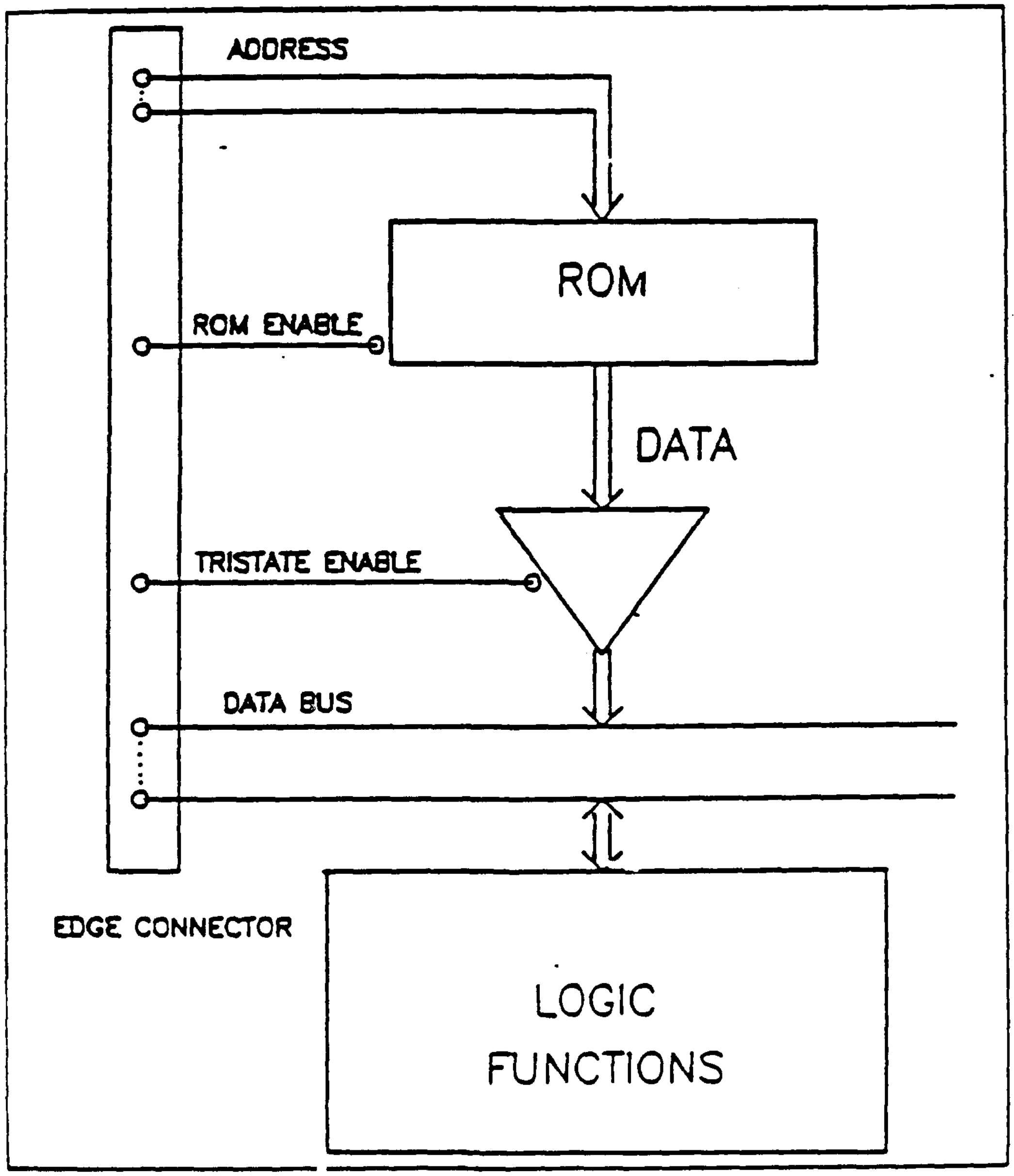


Figure 7-11. Control of Bus Logic Driven by ROM

7.4.3.4 Unused Logic Inputs. Every unused logic input pin should be terminated high or low. An input pin termination prevents the pin from reading noise and propagating noise-induced level changes into the device. It is desirable to terminate these inputs through pull-ups or pull-downs as opposed to directly tying them to Vcc or Ground.

7.4.4 Feedback Loops. Feedback loops occur in most moderately complex circuits. Complex loops containing memory elements often have to be separated into ··¬'ts for fault isolation. by backtracking algorithms. Generally, all the nodes in a loop do not change state together. In some loops, troubleshooting difficulty arises when errors propagated through the loop are fed back to the beginning as well as to the edge of the board where they are first detected (Figure 7-12). Segmenting a loop does not normally require additional logic devices. The approach shown in Figure 7-12 is to use a gate in place of one of the inverters in the loop and wire the additional input through a resistor to Vcc as shown. This input can then be driven LOW by the tester in order to interrupt the loop. Controlled access within the feedback loops helps in identifying fault conditions, especially when the loop contains many ICs.

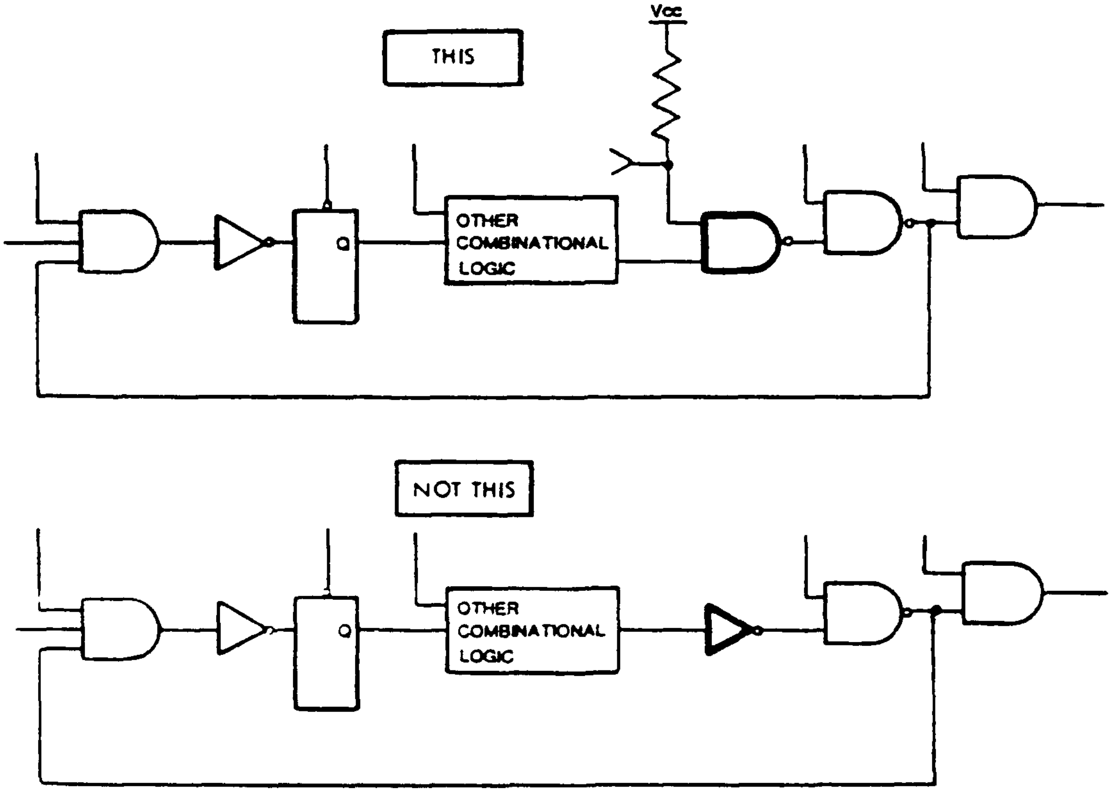


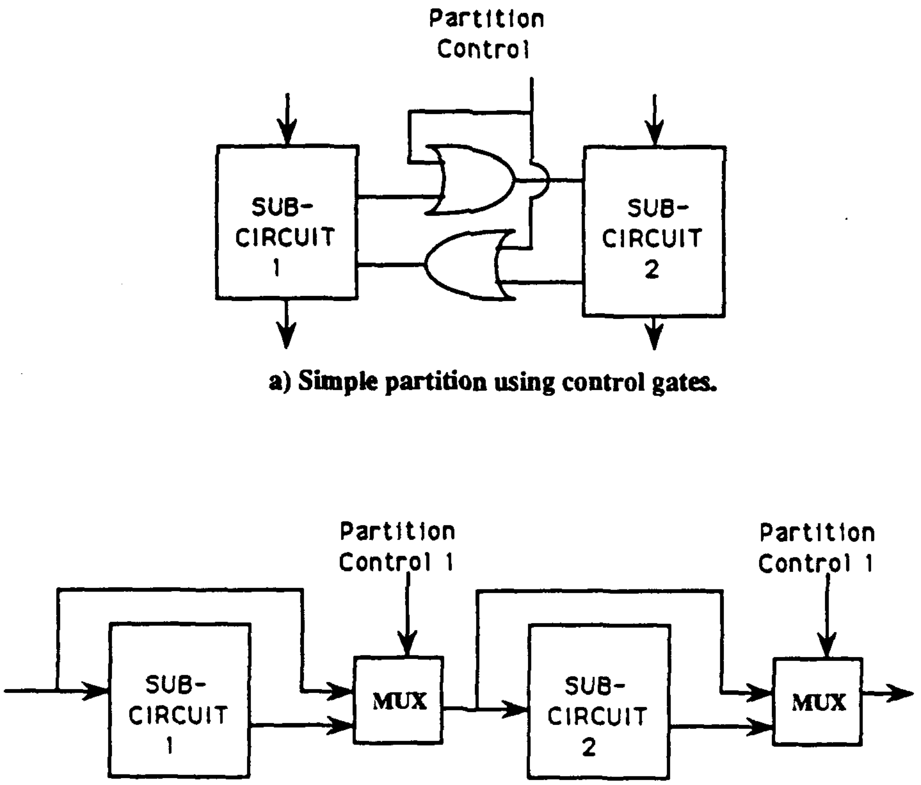
Figure 7-12. Disabling Feedback Loops

7.4.5 Partitioning. It is generally agreed that test generation costs are exponential and are non-linear in proportion to the size of a circuit. As a rule of thumb, the cost for an SSI/MSI circuit containing (n) devices is proportional to a number between n^2 and n^3. It follows that the cost can be drastically reduced if the circuit can be divided into sub-circuits that can be tested independently. For example, if n = 100 and assuming the best case square relationship, the reduction in cost for 5 sub-circuits each containing 20 devices is:

$$\begin{aligned} \text{Cost comparison (ratio)} \quad &= \quad (100)^2 : (20)^2 \times 5 \\ &= \quad 5:1 \end{aligned}$$

Partitioning can provide some serious cost savings! Lets look at how partitioning can be achieved and give some practical examples.

7.4.5.1 Implementing a Partitioning Scheme. To test each sub-circuit, all embedded sub-circuit I/O must be made available to the tester. Figure 7-13 illustrates partitioning schemes that can be used.



a) Simple partition using control gates.

b) Partition control using multiplexers.

Figure 7-13. Partitioning Scheme Examples

There are two basic types of partitioning: Hardware partitioning and Sensitized partitioning.

1. Hardware partitioning is achieved by inserting additional control gates, multiplexers, boundary scan, etc. that separate the embedded I/O of each sub-circuit to those primary circuit I/O points that are not being used by the sub-circuit under test. Additionally the partitioning scheme must prevent unwanted interaction between sub-circuits. On a bus structured board, partitioning is relatively simple by making the buses and associated tri-state control lines accessible at the primary I/O.

   For a non-structured board, however, additional circuitry may be needed to isolate the control clocks, resets and even power supply lines. This additionally circuitry can reduce the operating speed of the design and may be costly to implement. However, it may be possible to achieve the same results by the following method.

2. Sensitized Partitioning allows circuit partitioning and sub-circuit isolation by pre-conditioning "sensitized" paths from the primary I/O to the sub-circuit I/O. This method relies on existing gates in the design but may need additional control lines to create the sensitized paths. Figure 7-14 gives an example of this method.

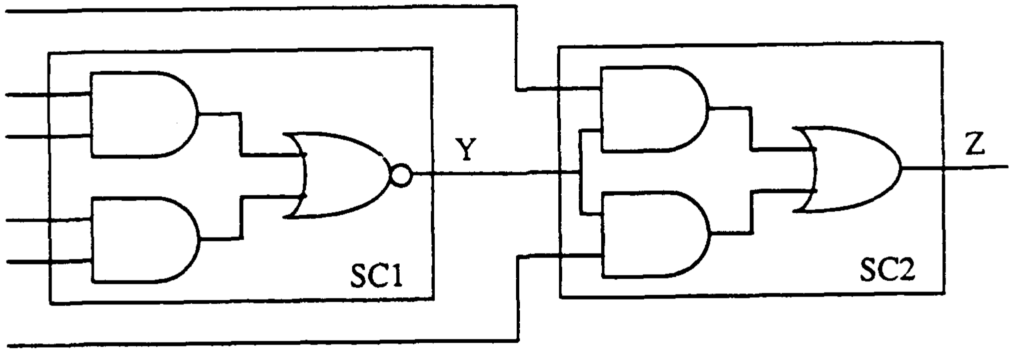


Figure 7-14. Sensitized Partitioning

The 6 input circuit in Figure 7-14 would require 64 (=2^6) tests to test the circuit exhaustively. By partitioning the circuit as two sub-circuits, SC1 and SC2, the tests can be reduced as follows:

1. Pre-condition a sensitized path for SC1 output Y by setting SC2 inputs A and F high. This makes the conditions of the pseudo-output Y visible at SC2 output Z.

2. Test SC1 using the 4 inputs; B, C, D, and E. 16 (=2^6) tests, required for this.

3. Pre-condition a sensitized input path for SC1 output Y by setting inputs B, C, and D low. This allows input E to control the condition of the pseudo-input Y.

4. Test SC2 using 3 inputs: A, E, and F. Eight $(=2^3)$ tests are required for this.

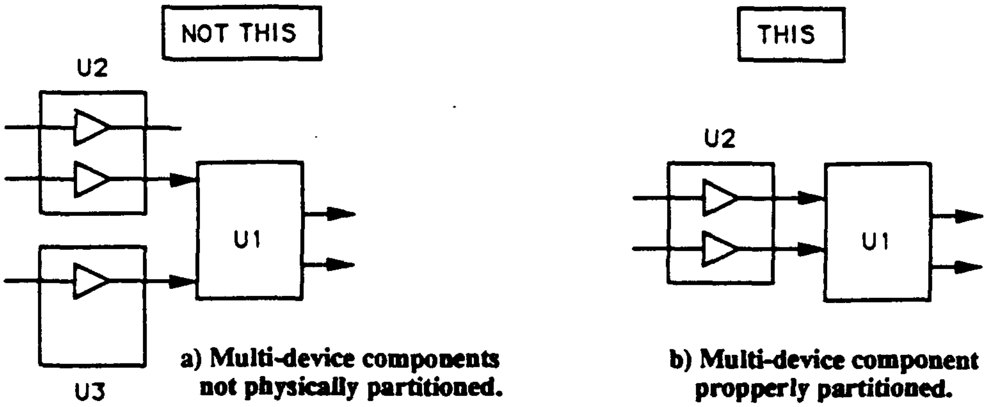
The circuit has now been tested for single stuck high, stuck low faults with 8 + 16 = 24 tests.compared with the 64 tests originally anticipated.

Although this example is simple, it does demonstrate the sensitized partitioning method. On a more complex design, great care must be taken to insure controllable paths that are insensitive to activity outside of the sub-circuit under test.

7.4.5.2 Physical Partitioning. All devices should be physically partitioned to facilitate test and fault isolation.

All components should be physically partitioned with at least 0.25 inches separating adjacent components. This allows for the use of test clip access during functional test.

All electronic devices which are contained within multiple device components should be partitioned in the same ambiguity group. (An ambiguity group is the smallest amount of devices that a fault can definitely be isolated to.) Therefore, if a failure occurs in the ambiguity group then less components need to be replaced. See Figure 7-15 where a failure in device U1 results in the inputs being replaced. The ambiguity group consists of U1 and the devices supplying inputs to U1.



a) Multi-device components not physically partitioned.

b) Multi-device component propperly partitioned.

Figure 7-15. Multi-Device IC Partitioning

7.4.6 Counter/Shift Registers. Several problems arise when counters or shift registers are used, especially if long sequences or chains are implemented. One problem is with initialization; another is the inability to control (via the ATE) the data input. Many patterns are long and complex, which complicates the test programs and verification of good circuits.

A third problem is not being able to control the clock input to a counter or shift register. Frequently the clocks are derived from complex on-board logic functions which also complicates the testing process and the writing of test programs. When on-board clocks are too fast for specific ATE, other techniques must be implemented to test these circuits. Cascaded counters or shift registers, which create long chains, can add to the problem of complex data patterns and test programs. These long chains increase the test time as well as adding to th~ test complexity. Counter stages or chains should be kept to a maximum of four stages without a break point.

The solutions to these problems are simple but may require several I/O pins and the addition of logic functions for implementation. Figure 7-16 illustrates the relevant techniques in an idealized solution for a combined counter/shift register. (The data paths shown can be serial or parallel).

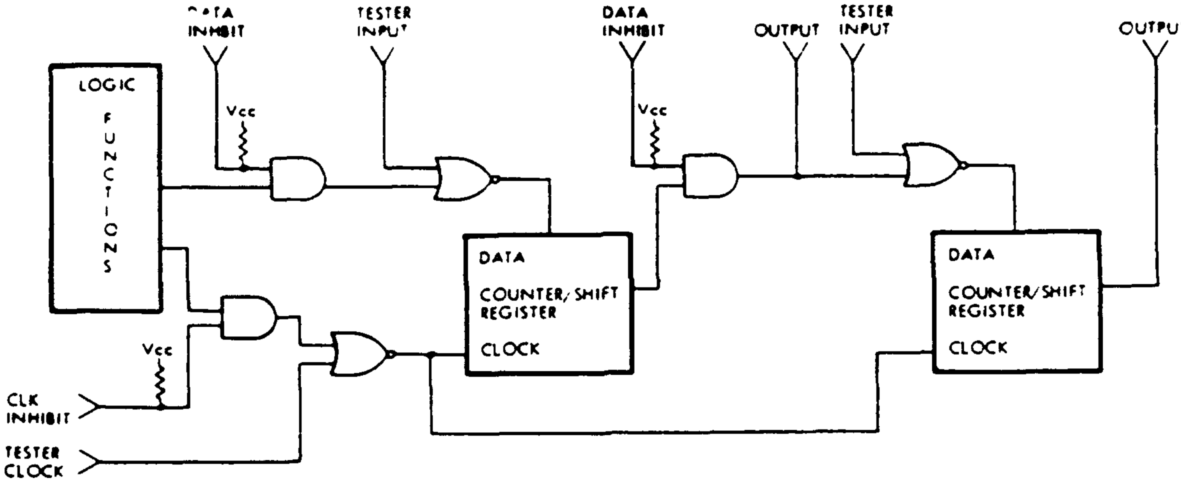


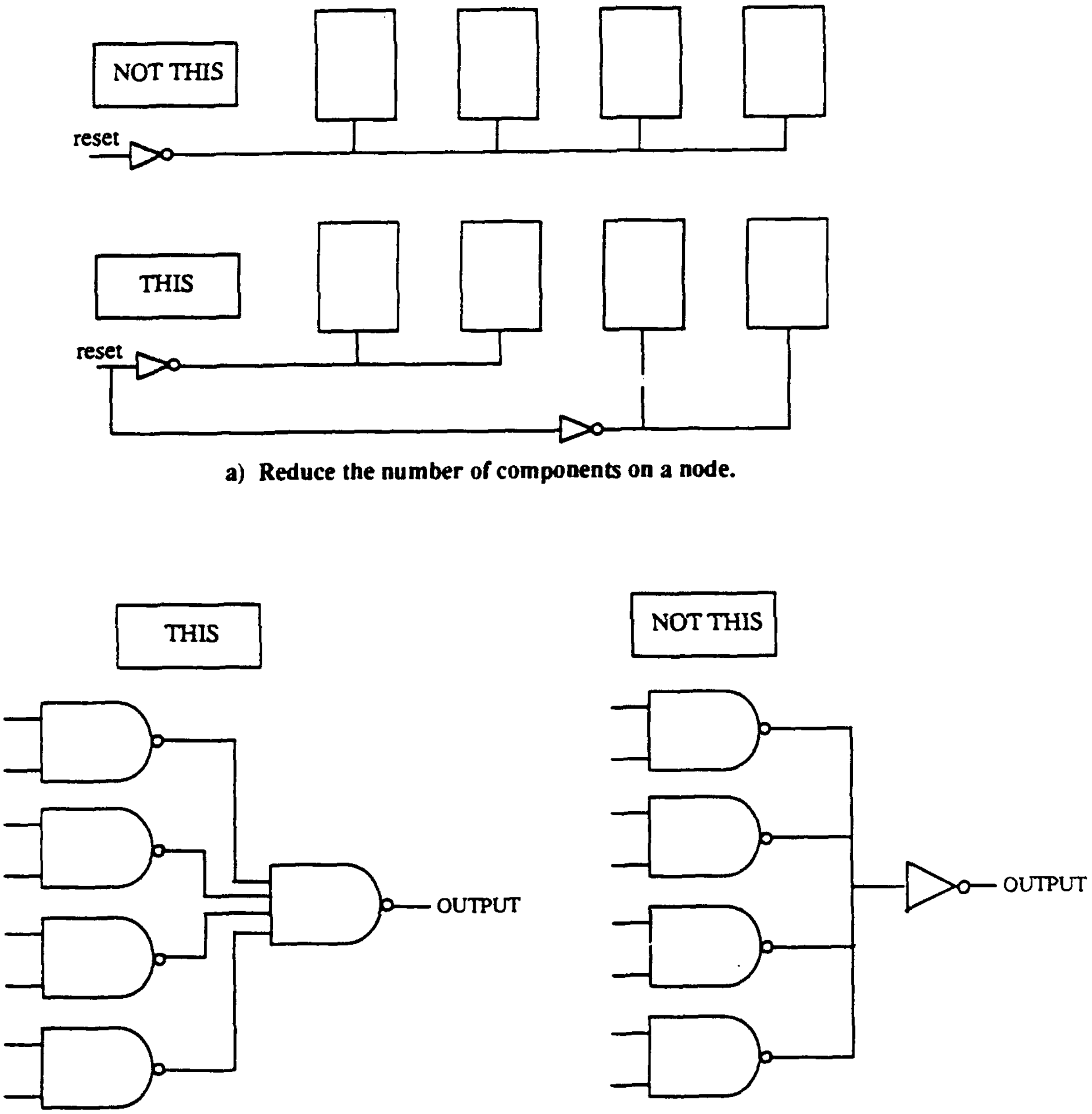
Figure 7-16. Combined Counter/Shift Register

As can be seen, the tester can now inhibit the on-board clock and supply a synchronized clrck of its own. This allows the tester to run at its own speed and control the operation of the registers. The tester can also inhibit the on-board data and supply its own data to each of the registers. This may or may not be a desirable feature depending on the particular test circumstances. The illustration also shows that a test point has been added to the output of each register and the chain between registers has been broken to allow each register to be tested individually, either with data provided by the tester, or from the previous stage. These are designer options.

Implementing such designs will allow circuits containing counters or shift registers to be readily tested without an excessive amount of test vectors. The tester also will be able to synchronize and control the test sequence rather than have to accept circuit control of the test.

7.4.7 Fault Ambiguity and Diagnostic Resolution. When diagnosing a failed UUT, the technician will ideally trace the fault to one device only. Unfortunately, most devices on a UUT are interconnected with other devices, which can cause a certain ambiguity about which device has failed. An 'ambiguity group' is the minimum group of devices that the diagnostic process can 'unambiguously' resolve for a specific fault. Further resolution of the actual failed device would need some physically intrusive troubleshooting such as cutting device leads or removing components. This type of troubleshooting is both costly and potentially damaging to the UUT and should be avoided if possible.

Typical ambiguity group diagnostic problem areas are wired OR/AND functions, high fan-out lines and bus-structured designs. Ways of avoiding these problems are shown in Fig. 7-17. It is also helpful to physically partition the circuit so that gates whose outputs are tied together are in the same package.



a) Reduce the number of components on a node.

b) Avoid Wired OR/AND functions

Figure 7-17. Test Point Availability on CCA

In the design of error detection circuitry, where many signals are ORed together to form a single fault indicator, a latching device should be provided for each signal input for fault isolation purposes as shown in Figure 7-18. The memory elements will aid a technician in determining where the error occurred, especially if the fault was an intermittent.

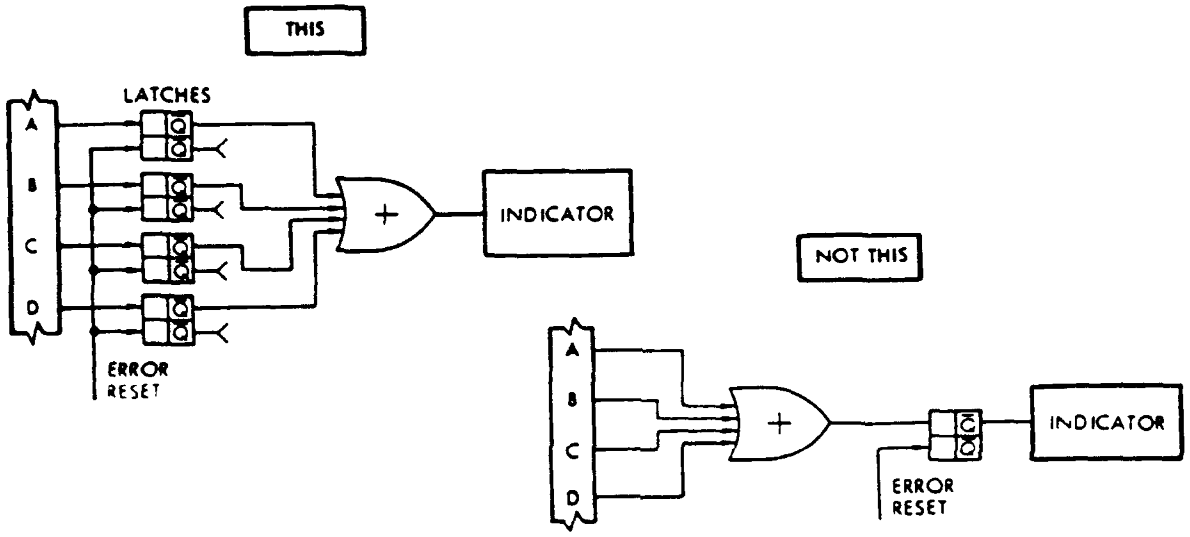


Figure 7-18. Added Memory for Fault Isolation

7.4.8 Asynchronous/Time Dependent Circuits. Any digital circuit functions that are asynchronous/time dependent can be a two-edged sword to the test process. On one hand, the UUT may not work correctly without the time dependent circuitry but on the other hand, asynchronous UUT activity may interfere with the test. The following sections identify some common problems and their solutions.

7.4.8.1 Refresh Circuits. Refresh circuits for dynamic memories (such as DRAMs) should be provided on the same board as the devices requiring it! However, the ATE must be able to control the refresh cycle directly to avoid undue synchronization problems with the test. This solves two problems: firstly, the ATE may not be fast enough to provide the refresh cycle, and secondly, the test software does not need to incorporate regular calls to complex refresh routines.

7.4.8.2 Watchdog Timers. Watchdog circuits that time-out and cause asynchronous events can be a nuisance during test. For instance, a microprocessor reset may be asserted if the microprocessor fails to stroke a watchdog circuit within a program dependent time period. In a similar circuit, a 'hung bus' condition may be asserted if no activity is detected on a bus over a certain time period. Adequate control and visibility given to the tester when designing these types of circuits enables the tester to:

1. Disable the time-dependent function so that it does not asynchronously interfere with the UUT test sequence and,

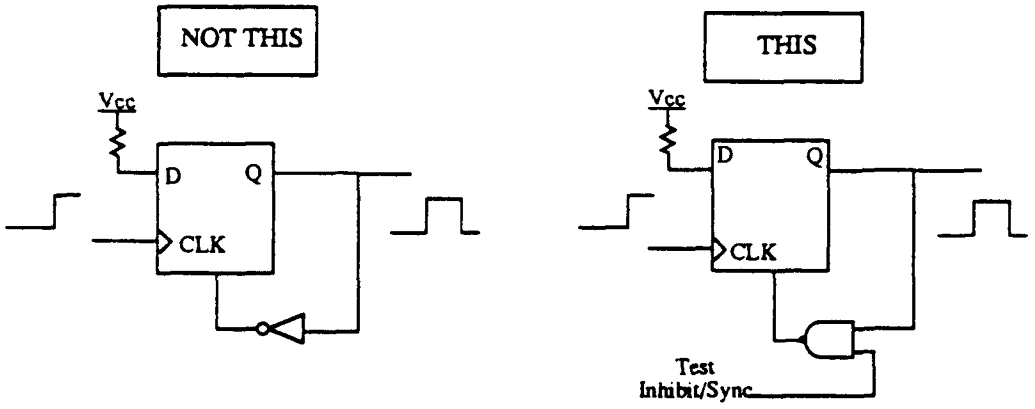
2. Control and monitor the watchdog circuit directly to confirm correct operation at an appropriate time in the UUT test sequence.

7.4.8.3 Asynchronous Logic. Asynchronous logic using latches and global feedback results in state transitions that are determined by the primary inputs only. No master clock is present to limit the speed of the state transitions which can be an advantage to the circuit design. However, various design techniques must be used to avoid glitches/race conditions, such as adding delay lines or logically redundant gates to delay signal propagation. The problem with this is that a faulty component may have no logical effect on the circuit but re-introduces a glitch or race condition that is not predictable in behavior (non-deterministic).

Not only would this cause problems with detecting/isolating the fault but also a deterministic fault simulator will have problems handling a circuit with non-deterministic faults.

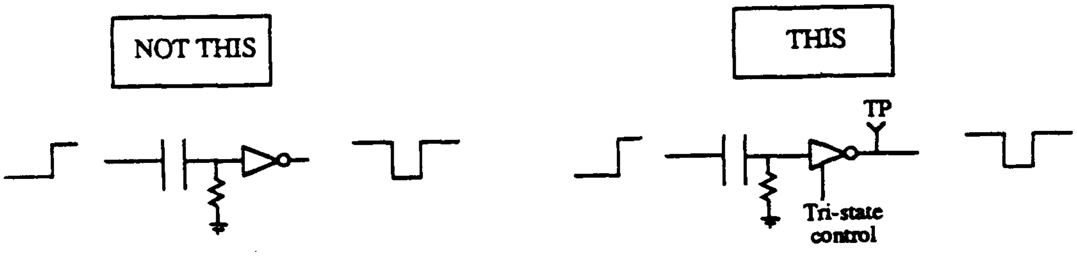
The answer to these problems is to avoid asynchronous logic wherever possible and preferably to use synchronous circuitry throughout the design.

Typical problems are shown in Figs. 7-19, - 20, - 21 and - 22. In these cases where asynchronous circuits have been used, the tester must be allowed to intrude into the circuit function and inhibit asynchronous/non-deterministic behavior.



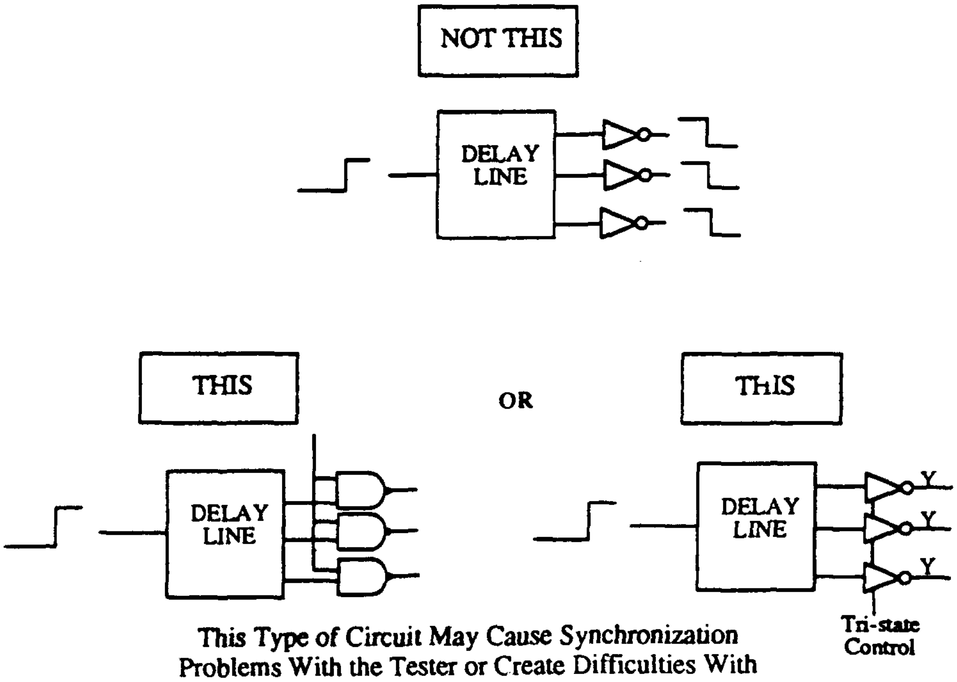
Added Control Allows Inhibit or Synchronization
by the Tester.

Figure 7-19. Self-Resetting Circuit



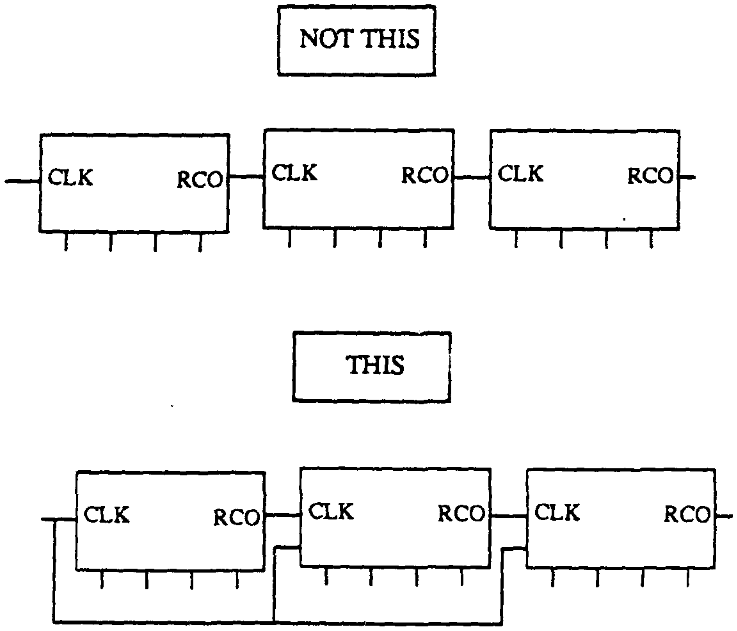
Tri-state Component/Test Point Allows Direct Tester Control/Visibility of Circuit Output.
(this type of circuit should generally be avoided)

Figure 7-20. RC Pulse Generation



This Type of Circuit May Cause Synchronization Problems With the Tester or Create Difficulties With Fault Simulation.

Figure 7-21. Delay Line Sequencer



Asynchronous Counters (or even asynchronously-coupled synchronous counter chains) Can Cause Race Conditions Leading to Difficult Test and Fault Simulation.

Figure 7-22. Asynchronous Counter chains

7.4.8.4 Monostables (One-Shots). The most commonly occurring asynchronous circuit is the monostable or one-shot. Unfortunately, these circuits are prone to output jitter and false triggering. Pulse width also varies with voltage, temperature and component tolerance leading to repeatability problems over the environment and from system to system.

Since all digital hardware should be designed to be frequency scaleable, one-shots (and delay lines) are to be avoided. However, if no other course of action is possible, a one-shot may be used, but only under the conditions described here.

Normally, one-shots designed into circuitry present an as;synchronous characteristic in their outputs which are difficult to observe and measure, and thus do not easily lend themselves to automatic testing. Testing of the one-shot and the driven circuit may need to be considered as separate steps in the test procedure depending on the ATE used. That is, the input and output of any one-shot must be made accessible to the ATE so that it can be tested in isolation. In addition, the output of the one-shot must be replaceable by the ATE to test the balance of the circuit. It is recommended that these points be brought out to the CCA connector or be otherwise made readily accessible by ATE as shown in Figures 7-23 and 7-24.

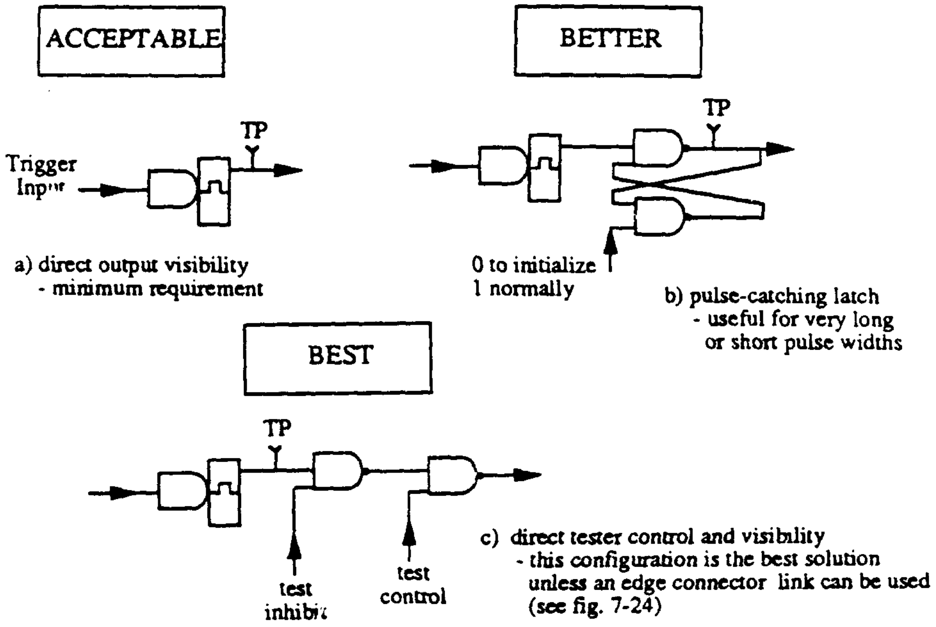


Figure 7-23. Design for Test Solutions for Monostables

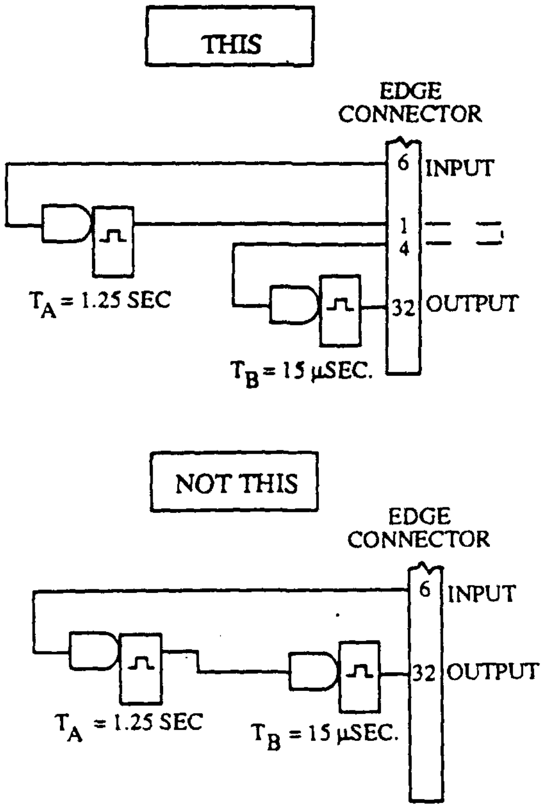


Figure 7-24. Improved Testability of Cascaded One-Shots.

SECTION 8. VERY LARGE SCALE INTEGRATION (VLSI) GUIDELINES FOR TESTABILITY

8.0 OVERVIEW.

This section discusses all Very Large Scale Integration (VLSI) devices other than microprocessors, microcontrollers, and memories which are covered in sections 9 and 10.

Semiconductor manufacturers are placing on the chip what used to be contained in an entire system. Industry statistics indicate that the number of devices per CCA is not decreasing. Rather, the number of functions per CCA is increasing in order to meet marketing and application demands. The result is that the average 100 IC CCA has drastically increased in complexity. As the complexity of assemblies increases, the cost to test them increases exponentially (see Figure 8-1).

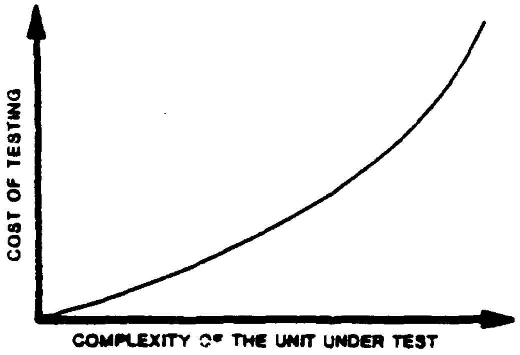


Figure 8-1. Complexity Vs Cost

When dealing with LSI (large scale integration) and VLSI (very large scale integration) logic, the SSI (small scale integration) and MSI (medium scale integration) guidelines do not go away. The guidelines for SSI and MSI circuits can be applied to the internal structure of LSI devices at the chip level. The testability guidelines build on each other and the fundamental concepts of synchronization, partitioning, initialization, control and visibility must not be ignored.

8.1 LSI Based CCAs.

8.1.1 Advantages of LSI Based CCAs.

8.1.1.1 Inherent Partitioning Dictates Tests Strategy. Because LSI devices have so much internal capability, they can be designed into a CCA in such a way that the CCA is inherently partitioned. It is important in designing for testability to take advantage of this feature. Once the LSI based assembly has been structured for partitioning, an effective testing strategy can be employed. The typical test sequence is as follows:

1. Verify that the address, data, and control buses are free from any stuck-at-one or stuck-at-zero faults. This is done using ATE and selectively tri-stating the drivers and receivers tied to their respective buses.

2. Allow the ATE to communicate, via the bus, with the microprocessor and run a few basic operation codes (see section 9, microprocessors).

3. The ATE should then check the ROM (read only memory). A check sum comparison is a good test of this section (see section 10 for more information).

4. If a self-test program has been written, the microprocessor can then be allowed to run the self-test and check the RAM (random access memory) and any remaining devices on the bus while the ATE is monitoring the test (see section 9 for more information).

8.1.1.2 Bus Visibility and Control. Another advantage of LSI based CCAs is that test points when provided on the bus are shared among many devices and provide access to all of them, one or a few at a time, through tri-stating techniques. This feature greatly reduces the fixture and interface requirements of the CCA to the ATE and maximizes the utilization of test points.

8.1.1.3 Self Test. LSI based assemblies containing both a microprocessor and on-board memory (typically ROM) have the advantage of being able to have self-testing capabilities. Self-tests are small resident programs, usually less than 2,048 bytes, provided on the CCA as a means of verifying that the CCA is performing all of its functions. The on-board test program can be used in conjunction with the ATE to generate multimillion pattern test programs with relative ease.

8.1.2 Disadvantages of LSI Based CCAs.

8.1.2.1 Sequential Complexity. By their very nature, LSI devices are inherently sequential; the entire PCB of yesterday has been implemented on a chip. Long counter chains and deep sequential networks are an integral part of each LSI device. Since the engineer designing the assembly has no control over the inner workings of the devices, testability becomes a problem.

8.1.2.2 Logic Definition Complexity. Another disadvantage stems from the fact that most LSI devices are designed to work within a bus-oriented CCA architecture. Because of this, most operate with three input/output levels - logic low, logic high, and high impedance (tri-state). Many of these devices also operate in three modes: drive, receive and off (tri-state). Where once it was always possible to ascertain the direction of signal flow based on the logic design, LSI devices complicate things by changing modes, over time, under control of software. One test axiom in the SSI and MSI world was to replace the driver first (most likely failure), and then the driven. LSI CCAs have a new problem - sometimes a chip is a driver, at other times it is a receiver. These new features greatly complicate the fault isolation process and are a major cause of increasing test costs.

8.1.2.3 Feedback Complexity. CCAs with LSI devices tend to create large hardware/software feedback networks. Events are caused to happen, say by a microprocessor, and later evaluated by the same microprocessor or pass-through software. The result of an event may be determined by a previous event, often internal to the chip. Again, since the design engineer has no access to the internal working of the chip, he has a testability problem.

8.1.3 LSI Failure Mechanisms. Another thing that the advent of LSI has provided is a new set of failure mechanisms. While the standard stuck-at-one/stuck-at-zero failure modes common to SSI and MSI devices still occur, a new set of failure modes has surfaced. These are called soft failures and include pattern sensitivity, timing sensitivity, noise sensitivity, and intermittent failures. This new set of possible faults has led to such new testing problems as the need for dynamic functional testing for operating the devices at or close to their rated operating speeds, and the need for very long (multithousand to multimillion step) test patterns, so that all possible fault conditions may be propagated to a point of visibility.

8.2 Visibility.

Visibility is the ability to externally monitor the internal operation of a unit under test. With SSI and MSI CCAs, the need for many test and control point exists (the rule of thumb being one test or control point per integrated circuit); with LSI based CCAs, the number of these points is reduced. Visibility to certain lines on LSI based CCAs is now more standard and more crucial. These include bus lines and status indicator lines.

The best access for visibility is through the edge connector or a test-only socket, since the speeds at which LSI based CCAs operate may preclude the use of IC clips or bed-of-nails fixtures. Access to keyboards and displays is especially important to eliminate human interaction and to reduce fixture and interface problems. Even with LSI based CCAs, all of the previous guidelines for visibility apply.

Increased visibility into a circuit increases the testability of an assembly in the following three ways:

1. Increased visibility reduces the amount of time and effort in the generation of test programs since fewer patterns are needed to propagate faults to a circuit node monitored by the ATE.

2. Increased visibility allows test programs to be executed in a shorter amount of time since fewer test patterns are needed to propagate faults to a node monitored by the ATE.

3. Increased visibility reduces the required number of operator probes during the fault isolation process. The majority of time in testing most LSI based CCAs, with typical failure rates and fault distribution, is expended during the fault isolation process. The probing sequence is typically software-guided by the ATE and prompts an operator to probe the required points on failing assemblies. Due to the high level of human intervention, this is a timely process and extremely prone to erroneous operator probes. In many cases the addition of one test point can cut the number of operator probes in half.

8.3 Controllability.

Controllability is the ability to externally (typically via ATE) alter the internal status of a unit under test. Control is imperative if the CCA is to be functionally testable. Control is especially needed over interrupt lines including those known as READY, RESET, HOLD, TRAP, and NMI (nonmaskable interrupt).

Figure 8-2 shows a small section of a schematic for a Z80 microprocessor based CCA. In this example, program control is passed to the ROM whenever a RESET or an INTERRUPT occurs. The normal operating program in this ROM services the interrupt request. During the testing process, control from the ROM is relinquished and given to the ATE. This allows the ATE maximum control and allows the test programmer to execute any special testing code deemed necessary without losing control of the CCA. In this example, the only way to initiate a reset is to cycle the power or to indirectly control, if possible, the SYSTEM RESET line directly with the ATE. This is needed not only to aid in the initialization process, but also to allow the chip select decode circuitry to be verified.

The improvements for testability are shown in figure 8-3. A three-input AND gate is used in place of the two-input gate. The third input is pulled high through a resistor and a control point is made available to the ATE. This allows the ATE to initiate a CPU reset with a single pulse. The now unused two-input AND gate can be configured as shown, allowing the ATE to electrically isolate the on-board ROM and data bus and emulate its function through added control points on the data bus.

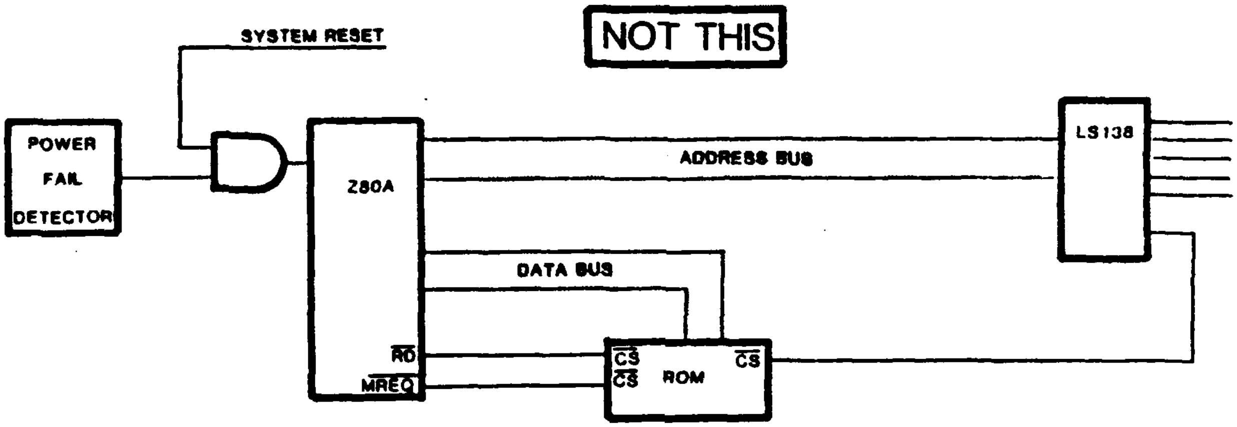


Figure 8-2. Interrupt Lines, Undesirable Controllability

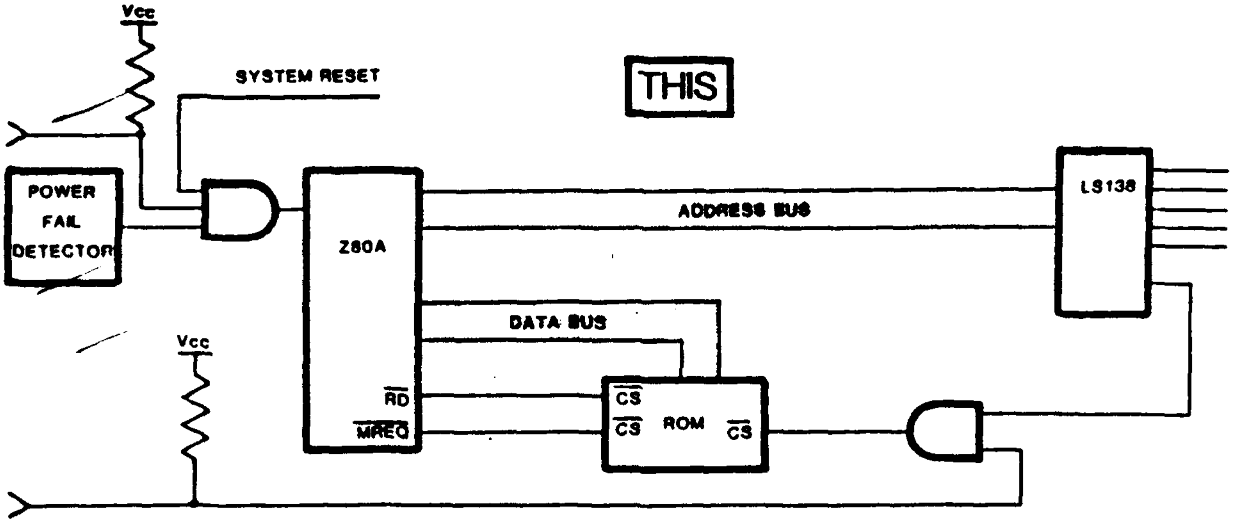


Figure 8-3. Interrupt Lines, Desirable Controllability

Control is of vital testing importance and has not been provided in the example shown in Figure 8-4. This is a section of a microprocessor-based CCA containing dynamic RAM and its associated refresh circuitry. As can be seen, no methods are in place for externally controlling the WAIT line. This line is important from a testing standpoint for two reasons. First, allowing control over the WAIT line will allow the use of an I/O rate determined by the test system for testing this CCA. The alternative would be to use a very expensive high speed synchronized dynamic test system, which may not be available. Second, if a failure occurs in the coniuol or refresh circuitry, random wait states could be generated, or worse, the entire system could be locked-up preventing quick fault isolation.

The solution to this testing problem is to use a three-input NAND gate in place of the two-input NAND (see Figure 8-5). The third input is tied to Vcc through a resistor and control over that input is made available to the ATE. Now, under program control, the ATE can disable the effect of the refresh and control circuitry and prevent any failures in this section from locking up .he system and hindering the testing of other sections of the CCA.

NOT THIS

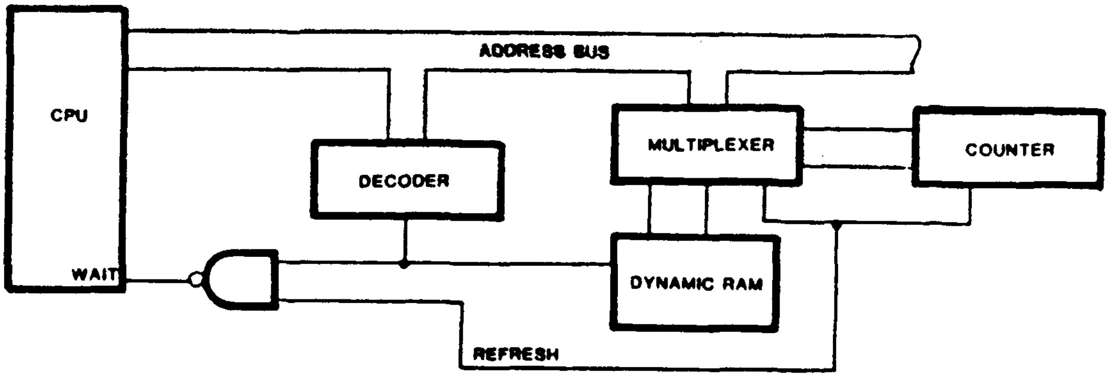


Figure 8-4. WAIT lines, Undesirable Controllability

THIS

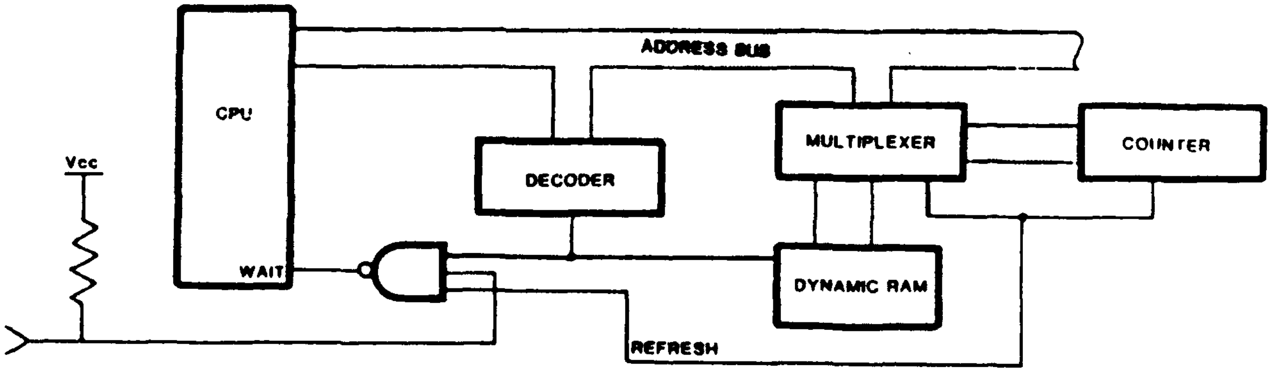


Figure 8-5. WAIT Lines, Desirable Controllability

As with SSI and MSI assemblies, edge connector access to the control points is recommended as a first alternative. As a minimum consideration, RESET and HOLD lines should be tied to Vcc or ground softly and allow for clip access when not used in the intended circuit function. A better testability practice is to bring these lines to the edge connector or to a TEST ONLY socket.

Additional control points increase testability of an assembly in three ways:

> First, increased control can greatly reduce the amount of time and effort in the generation of test programs. By having external control of a circuit, fewer patterns are needed to set up proper testing conditions and propagate faults to a circuit node monitored by the ATE.
>
> Second, fewer test patterns due to increased control allows test programs to be executed in a shorter amount of time.
>
> Third, increased control enables test partitioning which reduces the number of possible fault types during any given testing operation and allows for faster fault isolation. As mentioned earlier, the majority of time in testing most LSI based CCAs with typical failure rates and fault distribution is expended during the fault isolation process. A significant amount of that time is spent tracing the wrong fault either because of multiple faults per CCA or masked faults, which prevent accurate diagnosis.

8.4 Synchronization.

The unit under test and the ATE must be in synchronization with each other in order for testing and fault isolation to take place. This has recently become a major concern of engineers charged with programming ATE, primarily because many of the microprocessors are operating at frequencies higher than the ATE can handle. The more sophisticated processors include internal clock generators and do not lend themselves to external control for testing when configured as listed in the manufacturers' data books. Most dynamic functional testers operate only at 2 to 5 MHz and a few ATE manufacturers boast of speeds from 10 to 20 MHz. However, even with the 20 MHz tester, the fastest that data can be collected accurately is 10 MHz.

Certain types of faults are best diagnosed at specific speeds:

1. manufacturing faults at slow speed (static tesL).
2. pervasive timing faults at controlled dynamic (single- stepped) speed.
3. subtile timing or design faults at free running speeds.

With access to the READY and HOLD lines, the speed of the microprocessor can be controlled by the tester. Thus allowing single stepping or microprocessor-isolated testing. With control of on-board clocks or access to on-board sync, the use of high speed ATE with external synchronization capability can be used to test at normal circuit operating speeds.

8.4.1 Clocks/Oscillators. Clock lines should either come from the CCA edge connector or be enabled via control points activating logic inserted between the clock and its eventual destination or be designed to be disabled and overdriven (see Figure 8-6).
In the case of on-chip clocks, buffer circuitry should be provided on the CCA to provide the ATE with a synchronization signal. If left unbuffered, connection of the ATE to the unit under test may cause the CCA to cease to operate.

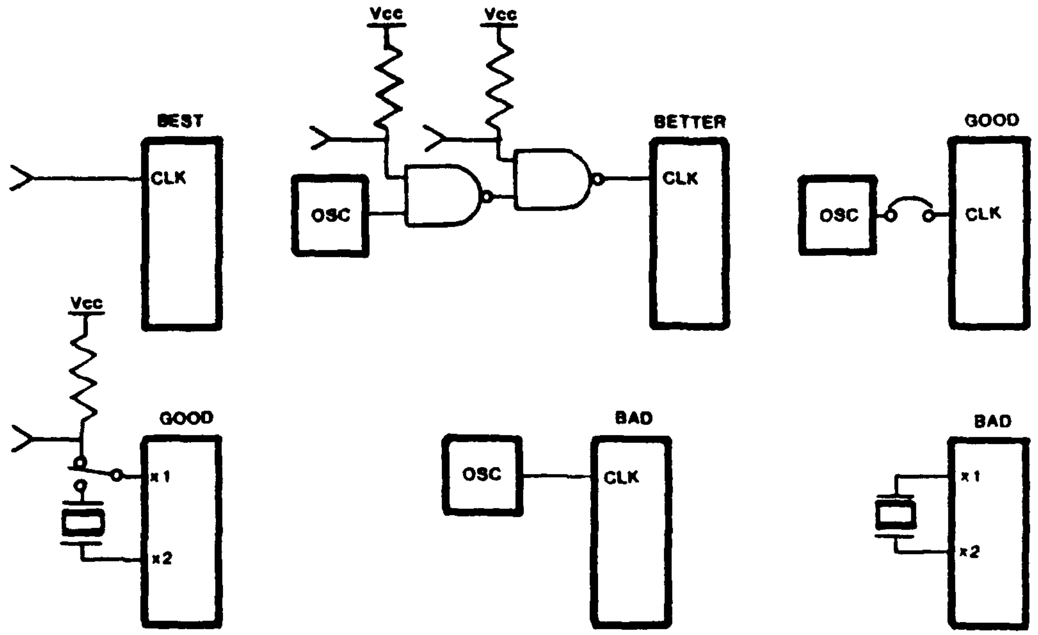


Figure 8-6. Clock Synchronization

Often LSI based systems require more than one on-board clock. These clocks may not have to synchronize to one another from a functional approach. However, multiple clocks can cause tremendous testing problems from all three testability standpoints - program generation, test execution, and especially fault isolation. If multiple clocks are required in a particular design, it is recommended that all lowe: frequency clocks be derived from one master clock. Do not use multiple free running clocks if at all possible and remember to allow for master clock input/ enable/disable as well as resets for the divide-by-N counters.

It is crucial that there be synchronization between the unit under test and the ATE. This synchronization must be predictable and repeatable.

8.5 Initialization.

Initialization is the process of getting memory elements on a logic circuit board into a known state. Digital testing and fault isolation cannot begin unless the unit under test is first initialized. Just as initialization was required for SSI and MSI, LSI requires initialization also. However, most LSI devices have internal memory elements that can be initialized only through software. Any fault that precludes initialization of the unit under test cannot be diagnosed with the ATE.

An important testability element that has been provided by LSI technology is the requirement for software initialization. Software initialization requirements come about due to two factors. One is that LSI based CCAs are inherently sequential. The other is that access to the logic elements internal to an LSI device that require initialization cannot be achieved via hardware means. The problem is compounded when an interrupt is serviced prior to software initialization. This interrupt may be generated as a result of an uncontrollable PROM routine, the result being that unknown states are propagated throughout the CCA. This precludes synchronization by the ATE. Adequate visibility and control points will allow a test program to perform software initialization.

8.6 Partitioning.

Allow isolation of board subsections for partitioned testing. The most difficult job in partitioning a microprocessor board for fault isolation is sectioning the bus. If the bus is not functional, nothing will operate. If the microprocessor and other chips that normally drive the bus can be put in a high impedance mode, or tri-state, and if tester access to the bus is provided, the bus can be tested as an entity. Board partitioning makes a complex testing task possible by allowing the test program to be sectioned or structured. Testing can then be applied on bus-structured boards with inherent chip enabling.

A well-structured testing philosophy is contingent upon being able to partition the LSI based assemblies under test. The advantages of tri-state conditions and the inherent partitioning of LSI based assemblies are completely lost if the CCA is designed with these lines tied hard to a power or ground bus. The best way to allow use of these lines and not affect the intended functionality of the CCA is to tie unused lines softly to power and ground buses and, at the very least, use a jumper plug to allow external control of these lines. Tri-state control lines should be made controllable by the ATE wherever possible.

Partitioning is an effective technique for breaking feedback loops and provides a means to isolate faults within those loops. Single board computer architectures typically have large feedback loops formed through the address and data bus. Any error would be easy to detect because all data streams within the loop would appear to have erroneous data. However, the fault isolation would be very difficult. Refer to Figure 8-7.

Figure 8-8 shows a method for breaking the classic single board computer feedback loop. This can be accomplished at either the address or data bus. In this example, an AND gate is added to logically AND the BUS REQUEST line with a control signal from the ATE. By pulling the control line to a logical low, the tester may tri-state the bidirectional buffer, breaking the feedback loop. This will allow quicker and easier fault isolation.

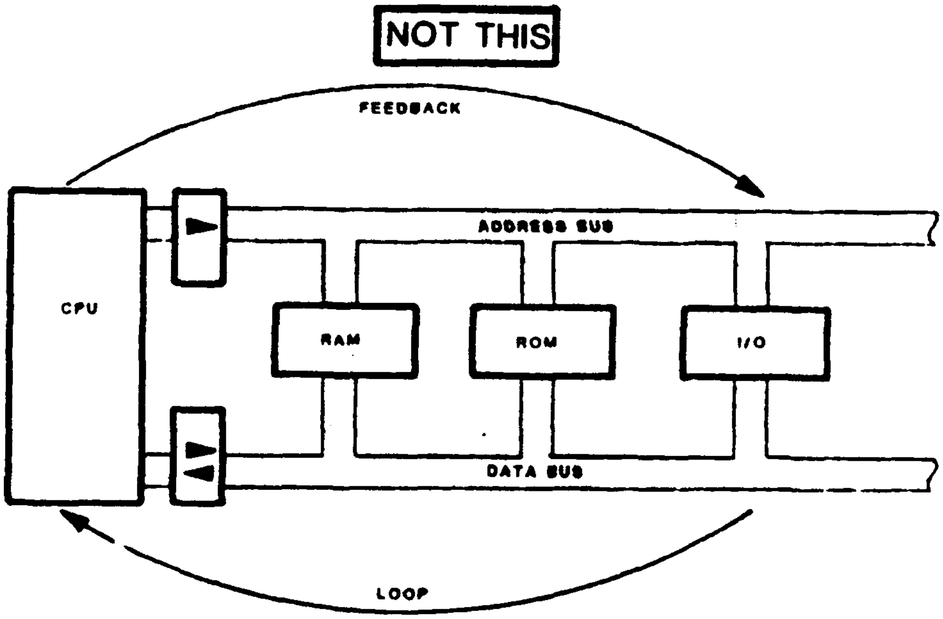


Figure 8-7. Undesirable Partitioning

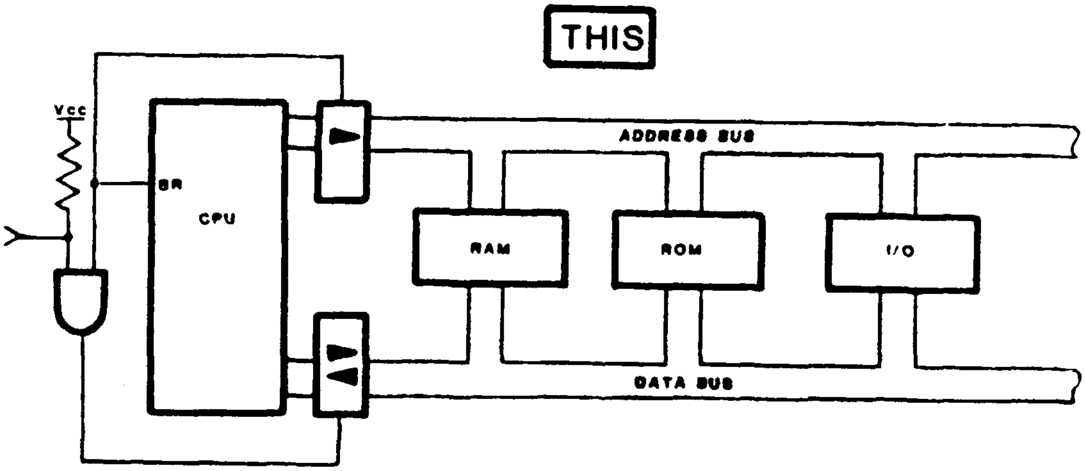


Figure 8-8. Desirable Partitioning

8.7 Self-Tests.

Mention was made of multimillion pattern requirements for thorough testing of a complex LSI based CCA. To generate this, many patterns for an ATE program is a formidable task. But the on-board PROM (1K or 2K) can take advantage of the microprocessor to help generate multimillion pattern test programs quite easily. The key from a testability standpoint is to make sure the test engineer can take advantage of the self-tests (For more information, see section 9 on processors).

Self-tests are generally designed to perform go/no-go testing of the assembly in which they are resident. As more CCAs become equivalent to complete systems, they will benefit from (or require) self-tests.

In addition to providing system go/no-go status, properly designed self-tests can reduce the test programming effort considerably. A well-designed 2K self-test in ROM reduces the test engineer's job to controlling the flow of data rather than generating a multitude of unique data.

The general guidelines for self-tests include structuring for partitioning and writing standard routines. When many CCAs use like devices configured in substantially similar ways as the kernel of the CCA, which may have a totally different function of input/output structure, use self-test routines that are transportable from CCA to CCA for the devices used. This reduces the proliferation of self-test programs and simplifies the design engineer's job. Many self- test programs need not be reinvented for each new CCA.

8.8 Device Standardization.

Testability is greatly enhanced when multi-processor CCAs use similar or, even better, the same devices. The test program generation effort is considerably reduced by the ability to use similar, or the same, program modules (from the same manufacturer) for multiple devices.

LSI devices take a long time to fully characterize. Avoid the temptation to use the LATEST and GREATEST. It may not work, it may not be available long term and it may not be documented properly (especially from foreign manufacturers).

Specifications for SSI and MSI devices are easy - fan in, fan out, propagation delay, etc. Specifications for LSI devices generally follow similar formats but the devices are orders of magnitude more complex. An idiosyncrasy that means nothing as far as the product performance from a design standpoint can cause nightmares in board test.

8.9 Standard LSI/VLSI Guidelines.

Most testability guidelines for modules can be adapted for applications using LSI/VLSI devices.

1. Divide long sequential state chains into several smaller chains, since those which are not controllable within a VLSI device complicate testing and test generation.

2. If a VLSI circuit does not generate a definite output for a given input during a functional test it becomes impossible to check the output against a known response.

3. Provide direct access to all VLSI pins Avoid sequential circuitry between VLSI pins and test points of connectors. This is due to the fact that sequential outputs need a "series" of test vector inputs and not just one.

4. Functions of custom design devices, such a s application specific ICs (ASICs) should be designed so that separate SSI devices do not need to be implemented with the ASIC on a board to complete the function or the ASIC. An example of this is an ASIC requiring pull-up resisters for signal integrity, these pull-ups could be designed in the ASIC and not require separate resistors. This could also decrease the ambiguity group since the pull-up resistors are not a separate device when they are integral to the ASIC.

5. Some CAD database are compatible with software which can automatically generate test vectors for a circuit design and analyze the thoroughness of the test vectors while reporting any testability design problems. Such a tool is very powerful and can greatly reduce the effort of test pattern generation. This tool should follow either the the waveform and (test) vector exchange (wave) specification EDIF 2.3 or 3.0.0 specs.

6. Provide VLSI documentation including any memory maps and a description of the device function.

8.10. Structured LSI/VLSI Testability Design.

Structured testability design implies that circuitry, specifically to improve testability, was designed into a device. The most common form of structured VLSI design is through the use of a scan technique. Scan technics use Shift Register Latches (SRLs) which can act as a normal register during functional operation, or can act as a shift register for retrieving or loading data to and from the register. Scan techniques are described in detail is Section 11 - Structured Design for Test.

Other structured testability techniques used in VLSI include Built-In Logic Block Observation (BILBO) and Signature Analysis:

1. The BILBO technique takes the scan path and LSSD concept and integrates it with the signature analysis concept. The end result is a technique for BILBO.

2. Signature analysis is often used as an adjunct to several testing methods including in-circuit and functional and serves basically as a data compression technique.

For more information on these techniques see Section 6 - Built-in Test.

SECTION 9. MICROPROCESSORS AND SUPPORT CHIPS.

9.0 OVERVIEW.

The following paragraphs cover many different microprocessors and several of the most frequently used peripheral chips. First, a general discussion is given on general microprocessor testability guidelines with a summary of the most popular processors in the market. Then, microprocessors are broken down into several categories and the most popular processors in each category are presented.

Each device is briefly described and its pin-out illustrated. It is then examined with respect to clocking and synchronization to the ATE system, initialization (hardware and software, where applicable), data evaluation by the ATE, and any special considerations particular in the use of the specific device.

Testability of microprocessor support chips is discussed in the final two paragraphs of this section.

9.1 Introduction.

Since a microprocessor board is, in many cases, a complete product, it is usually not too difficult to write a small routine to self-test a Printed Circuit Board (PCB). However, the ATE system's speed usually restricts the ability to effectively handshake with a microprocessor board running at rated speed. It is important, therefore, that timing relationships be fully understood and taken into account, especially from a diagnostic standpoint. In addition, a self-test routing proves out a good board but has difficulty in isolating faults, especially if the microprocessor kernal is dead.

Common to most of these devices are some general guidelines, which cannot be over emphasized. These guidelines include:

- Control of clock lines
- Access to the address and data buses
- Access to the SYNC or equivalent function
- Access to the RESET, HOLD and INTERRUPT lines
- Control of all tri-state devices
- Control of shift select lines
- Providing pull-up resistors on all tri-state buses
- Partitioning static devices from clock circuits
- Partitioning analog circuitry sections.

Perhaps the most effective testability design technique with any LSI/VLSI based board is to provide a self-test in ROM (or a separate ROM, which may be installed for testing purposes). Alternatively, using an Automatic Test Pattern Generator (ATPG) system to emulate the ROM allows complete control of the board under test. This technique can also make use of the power of the microprocessor to generate many test sequences with relatively few test program steps.

NOTE: In this section, inverted logic signals are represented by lines over the signal names or a slash '/' preceding the signal name. A signal with two names, one of which is inverted may appear as follows - NAME1/(not)NAMWE2.

9.2 Microprocessor/Microcontroller Testability.

Successful design for testing of a microprocessor/microcontroller requires that the circuit has been designed in such a way that maximum use of testability concepts such as control of the inputs and observability of the outputs has been made.

Presently there are literally hundreds of microprocessors/microcontrollers on the market with as many as half a dozen being introduced each month. Since the introduction of the original 4004, 4-bit microprocessor in 1971, we have come a long way with design of processors that provide "VAX-power-and-speed" to desk-top computers at reasonable prices.

Certain types of 8-bit microprocessors have become obsolete already including the 6800, the 8080, the 6501, etc. However, some 8-bit processors (such as the 6805 or the 8051) are still being used as controllers embedded in cars, appliances, etc. The 8-bit processor is by no means obsolete. Recently an 8-bit microcontroller was introduced using a RISC (Reduced Instruction Set Computer) architecture running at 20 MHz. Ninety percent of the 1988 commercial market of all microprocessors/ microcontrollers unit volume was made up of the 8-bit microprocessors. In 1987 alone Mitsubishi was averaging 40 million microcontrollers of the 50740 class (6502 core microprocessor).

Since most military electronics and other high tech. products tend to use the higher performance architectures, the 8-bit processor will only be covered briefly.

9.2.1 Microprocessor Testability Guidelines.

The following set of guidelines apply to most microprocessors and support chips. These guidelines are placed into five sub-categories entitled Accessibility, Controllability, Initialization, Synchronization, and General Guidelines.

9.2.1.1 Accessibility.

1. Ideally all internal buses should be accessible. Including data, address, and testability buses.

2. Include access to sync outputs (such as address and data strobes).

3. Be able to partition analog and digital sections for separate testing. Partition the circuit into smaller functional blocks (see section 8).

4. Non-multiplexed address/data lines on processors make for easier testability.

5. Be able to socket the microprocessor/microcontroller.

6. If unable to socket microprocessor/microcontroller (military applications) provide a test socket (empty) next to microprocessor/ microcontroller or provide a test connector to outside of UUT. Additional circuitry is often required to disable the on-board processor and to allow ATE control through the test socket. Adding a test socket to a microprocessor/microcontroller system needs more questions to be asked such as:

   a. Is the additional manufacturing costs of extra circuitry outweighed by savings in system repair and test time?

   b. How will the additional circuitry affect system reliability?

   c. Can the clock output drive two microprocessors/microcontrollers at once?

7. Provide a means to loop all processor CCA outputs back to the inputs (by means of an extra test connector , for example, using a test adapter). This provides a quick and effective CCA I/O test.

8. Provide space for test clip access (usually about 1/4 inch between ICs) to facilitate use of external instruments such as logic analyzers.

9. Always provide for electrical and mechanical interfaces to microprocessor signals for emulator access.

10. Provide a means for external equipment to be able to identify a microcode location if the microprocessor stops on an error.

11. BIT SLICE microprocessors should be separated into elementary slices for independent testing.

9.2.1.2 Controllability.

1. Be able to control chip select and output enables, including bidirectional buffer circuits direction lines.

2. For any UUT design with microprocessor and a memory always leave enough space in "on-board" memory to be able to load memory with a test program. This means access to loading of memory needs to be provided through an edge connector.

3. Provide control of the chip RESET, WAIT, HOLD, SINGLE STEP, and INTERRUPT type lines.

4. Include pull-up resistors on all tri-state lines.

5. Provide a means to control all tri-state devices/lines even if it means adding extra circuitry buffers (see table 9-1)

Table 9-1. Common Microprocessor Control Lines for Tri-states

INPUT LINES CAUSING TRI-STATES			NON-TRISTATABLE LINES/MP
Microprocessor	Input Line	Affected Lines •	Non Tristatable Lines
Z80	$\overline{\text{BUS RQ}}$	$\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, MREQ	$\overline{\text{MI}}$, $\overline{\text{HALT}}$, $\overline{\text{BUSAK}}$
6800	HALT	R/W	BA, VMA
6809	$\overline{\text{HALT}}$	R/$\overline{\text{W}}$	INTE, BA, BS, E, Q
8085	HOLD	$\overline{\text{RD}}$, $\overline{\text{WR}}$	$\overline{\text{INTA}}$, CLK, SOD, ALE, SO, S1, HLDA
8086	HOLD	$\overline{\text{BHE}}$/S, $\overline{\text{RD}}$, M/$\overline{\text{IO}}$(S2) WR, DT/R(S1), DEN(SO)	$\overline{\text{INTA}}$, HLDA, ALE
8088	HOLD	$\overline{\text{DEN}}$(SO), $\overline{\text{RD}}$, IO/$\overline{\text{M}}$(S2), WR, DT/R(S1)	$\overline{\text{INTA}}$, HLDA, ALE
68000	$\overline{\text{HALT}}$	$\overline{\text{AS}}$, $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, R/$\overline{\text{W}}$, VMA, FCO, FC1, FC2	E, $\overline{\text{BG}}$

• INCLUDES ADDRESS AND DATA BUSSES IN EACH CASE

9.2.1.3 Initialization.

1. All processors need to be provided with a restarting sequence in case they hang up due to an incorrect sequence.

2. Develop self-test programs for the microprocessor that can be stored in the ROM and initiated automatically during power-up.

9.2.1.4 Synchronization.

1. To properly sync ATE to processor clock speed, minimum clock speed of processor needs to be known.(i.e.,most of todays advanced 32-bit processors can attain speeds beyond present day ATE. Manufacturing Faults are best diagnosed at low speed, pervasive time faults at single step speed and subtle timing or design faults at free running/operating speed for given design.

2. Be able to control clock/oscillator lines (internal/external).

3. Be able to synchronize ATE to microprocessor/microcontroller. (Predictably and repeatable?)

4. All frequencies required to run microprocessor or subsets from one master oscillator should be available.

5. Provide a means to test any clock oscillator on a UUT immediately after power-up.

9.2.1.5 General Testability Guidelines.

1. Unused microprocessor control lines should only be tied to power buses through resistors or inverters, preventing shorting of power lines if microprocessor is defective. (This also ..lows a standard library test to be run if using an incircuit tester.)

2. When designing multi-processor configurations, use microprocessor from the same family and manufacturer for easier testability. This includes using support chips from the same family also.

3. All processors should be second source..

4. Full documentation should be available on all microprocessors and microcontrollers.

5. Select processors that have well-documented testability features.

6. UUT microcode should be available in a flow chart. (Including a memory map.)

7. Remember, designing a processor based module for testability has to be done in such a way that module malfunctions can be quickly isolated to either HARDWARE, FIRMWARE or SOFTWARE.

The thing to remember when designing a UUT with a microprocessor, memory, etc., is that the point of diagnosing a UUT problem is to isolate the failing circuit/sequence. In order to do this, it is essential that the UUT/SYSTEM have a modular partitioned design to start with. If this is followed, relatively simple (read "low cost") tools can be used for testing and debugging one item at a time in a modular fashion.

One way to save many hours of testing and debug is to pre-check the processor and support ICs such as memory before they are used in an actual design layout.

This requires simulation or bread-boarding of the microprocessor 'kernal', i.e. the microprocessor, ROM, RAM, and support devices. With a simple layout, the power-up boot sequence can be analyzed and some simple diagnostic routines can be run to see how the parts play with each other. Using actual hardware allows the designer to compare I/O waveforms against the data sheets and so reduces the risk of timing problems on the final layout.

9.3 Microprocessor Classifications.

Microprocessor/microcontrollers are usually classified by the number of bits or data lines (order of size) but there are so many microprocessor/microcontrollers that a larger classification will be used as follows:

CISC microprocessor	=	Complex instruction set computers microprocessor (section 9.4).
RISC microprocessor	=	Reduced instruction set computer microprocessor (section 9.5).
Transputers	=	Designed for easy parallel processor hookups (section 9.6).
Microcontrollers	=	Contains a complete microprocessor and peripherals on one chip (section 9.8).
Bit slice processor	=	Used for specialized digital controllers (section 9.7).
DSP, etc.	=	Digital signal processor (section 9.9).
Future processors	=	64-bit processors and larger (section 9.10).

Table 9-2 gives a summary of some popular microprocessor/microcontrollers on the market as of 1990, cross-referenced with information for testability.

Table 9-2. Microprocessor Testability Information Chart Summary (NOTE: partial implementation is designated by parenthesis - '(x)')

NO. OF BITS	MFG	PART NO.	MULTIPLEXED DATA/ADDRESS BUS	CISC MICROPROCESSOR	RISC MICROPROCESSOR	SUPER SCALER MICROPROCESSOR ARCH	TRANSPUTER	BIT SLICE	SINGLE CHIP/EMBED. MICROCONTROLLER	TECHNOLOGY	MIL STD 1750A	OPERATING FREQ (MHz)	MILLION INSTR/SEC	2ND SOURCE	COMMENTS
4 BIT	SIERRA	COP 400		X	.	.	.	.	X	CMOS	.				
	AMD	2900, 29C00, 29G00							.	CMOS	.				
8 BIT	SIERRA	COP 800		X	.	.	.	X	X	CMOS	.	20			
	PIC	PIC 1600		X	.	.	.	.	.		.				
	INTEL	8048		X	.	.	.	.	X	CMOS	.			XX	
	INTEL	8051/8052	X	X	.	.	.	.	X	CMOS	.			XX	
	MOTOROLA	6804/6805	.	X	.	.	.	.	.	CMOS	.			XX	
	MOTOROLA	6801/6301/68 MC11	.	X	.	.	.	.	.	CMOS	.			XX	
	ROCKWELL	6500/1, 65C124, 50740	X	X	.	.	.	.	.	CMOS	.	2-4	.	XX	
	ROCKWELL	37700	X	X	.	.	.	.	.	CMOS	.				
	ZILOG	Z8, SUPER 8		X	.	.	.	.	.	CMOS	.	12		XX	
	TI	7000		X	.	.	.	.	.	CMOS	.	6		XX	
	INTEL	8085A/80C85		X	.	.	.	.	.	CMOS	.	5		XX	
	ZILOG	780		X	.	.	.	.	.		.				
		HD64180/Z180	.	X	.	.	.	.	.		.				
	ZILOG	Z280	X	X	.	.	.	.	.		.				
	MOTOROLA	6800/6802, 6809/6309		X	.	.	.	.	.		.			XX	
	COMMODORE	650X/65COX	.		.	.	.	.	X	CMOS	.	2		XX	
16 BIT	CMD	65C816/65C802	X	X	.	.	.	.	.	CMOS	.	6		XX	
	INTEL	8C96		X	.	.	.	.	.		.				
	NAT SEMI	HPC 16000		X	.	.	.	.	.		.				
		783X		X	.	.	.	.	.		.				
	NEC	V SERIES		X	.	.	.	.	.		.				
	INTEL	8086/8088, 80186/188	X	X	.	.	.	.	.	CMOS	.				8086 16 BIT/16 BIT BUS
	INTEL	80286	.	X	.	.	.	.	.	CMOS	.			XX	8088 16 BIT/8 BIT BUS
	HARRIS	RT X 2000	.	X	.	.	.	.	X	CMOS	.	25		XX	(IBM-PC = 8088)
	HARRIS	RT X 3000	.		(X)	.	.	.	X	CMOS	.			XX	
	HARRIS	RT X 6000 (3000 CMOS)	.		(X)	.	.	.	.	CMOS	.				
	ZILOG	Z800X	X	X	.	.	.	.	.	CMOS	.				
	MOTOROLA	68000, 8, 10, 12	.		.	.	.	.	.		.				
	NAT SEMI	32016		X	.	.	.	.	.		.				
	NAT SEMI	32 CG 16			.		X	.	X		.				
32 BIT	INTEL	80386	X	X	.	.	.	.	.	CMOS	.	33		.	
	INTEL	80486	X	X	(X)	.	.	.	.	CMOS	.			.	CLSC ARCM INCORP
	TI	340 X 0				.	.	.	.		.				SOME RISC IDEAS
	VLSI	VL86C0X0 ARM				.	.	.	.	CMOS	.	10	1 5		
	NAT SEMI	32032	.	X	.	.	.	.	.		.	30			(1ST 32 BITTER
	INMOS	IMS T212, T414, T800		X	(X)	.	X	.	X	.	.			XX	FOR II PROCESS)
	AMD	29300		X	.	.	.	.	.	CMOS	.				
	ZILOG	Z80,000		X	.	.	.	.	.		.				
	MOTOROLA	68020	.	X	.	.	.	.	.	CMOS	.	16 7	2 5		
	NAT SEMI	SERIES 32000	.	X	.	.	.	.	.	CMOS	.	10	1 5		
	AT&T	WE32 FAMILY	.	X	.	.	.	.	.	CMOS	.	14	3		
	INTEGRAPH	CLIPPER (C300)		.	X	.	.	.	.	CMOS	.				
	SUN MICRO	SPARC RISC (B5000)	.	.	X	.	.	.	.		.	80	65	XX	B5000 (6 CHIPS SET
	M COMP SYS.	MIPS RISC (R3000)	X	X	(X)	.	.	.	.	CMOS	.			XX	COSTS $3 300)
	AMD	29000 RISC	.	.	X	.	.	.	.	ECL	.	25	17		
	MOTOROLA	88 X 00 RISC		.	(X)	X	.	.	.		.			.	
	INTEL	80960 CA	X	X	.	X	.	.	X	CMOS	.			XX	4 INST/CYCLE
	NEC	V70			X		.	.	.	CMOS	.	33	66	.	3 INSTR/CYCLE
64 BIT +	INTEL	80860 (N10)	.	.	X		.	.	X	CMOS	.	40		.	1 INST/CYCLE
	INTEL	80860CA			.		.	.	X	CMOS	.			.	4 INST/CYCLE
	IBM	AMERICA			(X)	X	.	.	X	CMOS	.			.	5 INST/CYCLE
	.				.	.	.	.	.	—	.	.			PROPRIETARY
	HP/APOLLO	HP/APOLLO DN 10000			(X)	X	.	.	.	CMOS	.			.	2 INST SIMUL (FUTURE
	SIGNETICS	68070	X	X	.	.	.	.	X	CMOS	.	20		XX	RELEASE)
OTHER D.S.P		WORD SLICE					.	X	X		.				
	AMD	29000/400, 29C300					.		X		.				
		74AS8XX/74AS88XX					.				.				* 80486 = 80386 + 80387
	MOTOROLA	6000/6001					.				-				PMMU - 82385

9.4 Complex Instruction Set Computer (CISC) Microprocessor.

The term CISC covers all processors that are not RISC processors. Intel and Motorola are at the top in the microprocessor business and Zilog is a distant third ahead of National. Most of the 8-bit microprocessors have been cloned by other American and foreign companies under agreement to Intel and Motorola.

Only a few years ago, the Motorola 6800 series and the Intel 8080A were the most popular 8-bit microprocessors with their support chips. Today these chips are obsolete and have been replaced by more sophisticated 8-bit microprocessors that are based on the original designs with more advanced concepts.

9.4.1 8-Bit (CISC) Microprocessors. The following paragraphs give examples of testability of three 8-bit CISC microprocessors, the 6800 family, the 8085A and the Z80 family.

9.4.1.1 The 6800 Microprocessor Family. The 6800 microprocessor is an 8-bit, single power supply (+5V) device with an external clock. It is now obsolete but illustrates the various testability techniques that can be applied to similar but more modern chips in its class (i.e., 6502, etc.)

It has perhaps the simplest timing considerations of any of the MOS microprocessors covered in this section. This timing simplicity occurs because a clock cycle and a machine cycle are one and the same for the 6800. The pin-out for the device is illustrated in Figure 9-1.

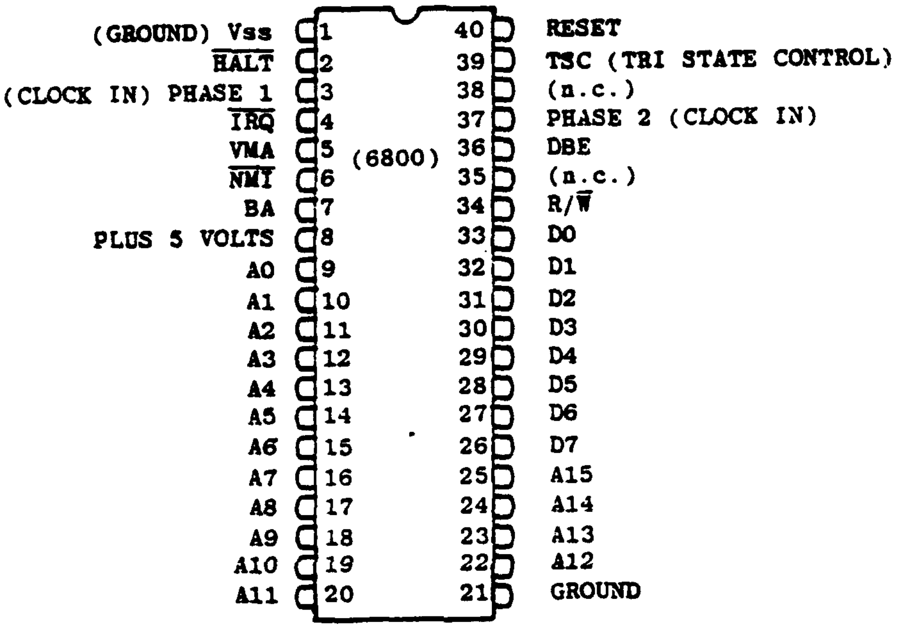


Figure 9-1. 6800 DIP Pin-Out

Tri-state control for the data and address buses of the 6800 has been split, with TSC (three-state control) providing for floating of the 16-bit address bus, and DBE (data bus enable) performing a similar function for the 8-bit data bus.

A third line, /HALT*, floats the entire system bus (address, data and the R/(not)W output), and causes the CPU to stop execution when the currently executing instruction has been completed.

* NOTE: Throughout this section signals which are active low are represented by one of three symbols - '/', '(not)', or by a line over the signal name.

One of the key guidelines from both testing and system design standpoints, is that RESET must be held at logic 0 for at least eight clock cycles (both for the powering up and during an in-process reset). From a testability standpoint, the preferred methods for accomplishing this are shown in Figure 9-3, in decreasing order of preference.

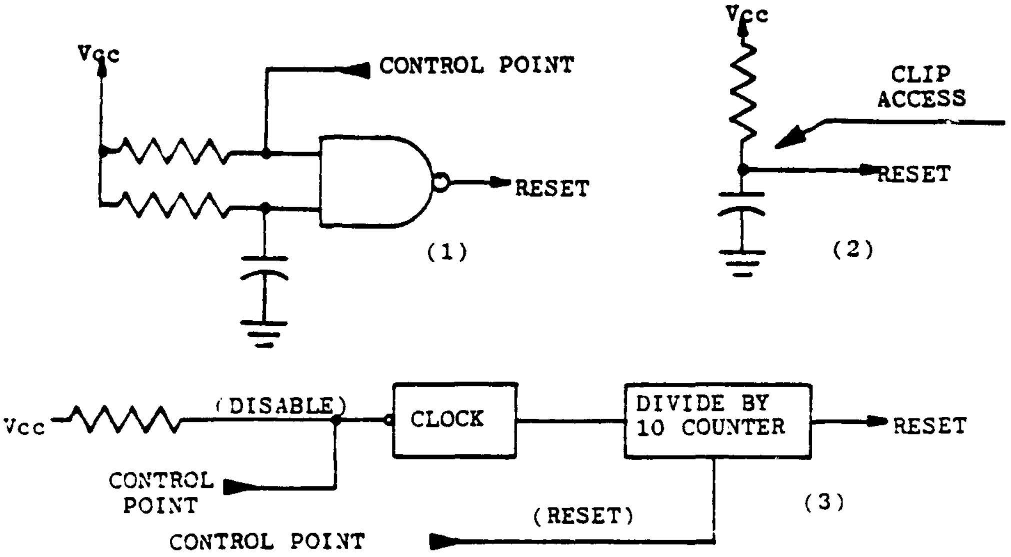


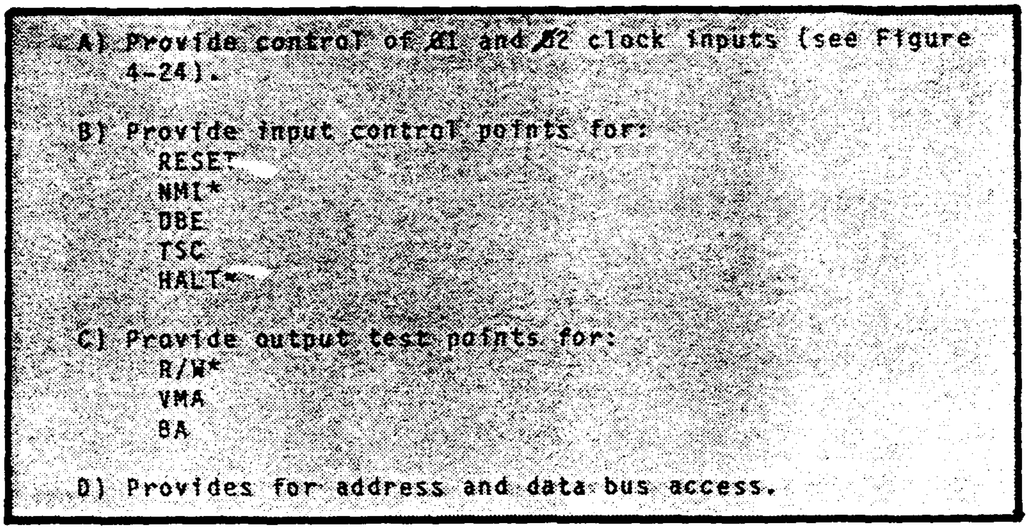
Figure 9-2. 6800 Reset Control Methods

Method (1) is a compromise between method (2), which needs fewer parts but requires clip access (or an edge connector access, in which case it is the preferred method) and method (3), which requires more components.

After a reset operation, the 6800 will load from hexidecimal addresses FFFE and FFFF. Provision should be made to allow the CPU to access the ATE system at these memory locations, so that the test system can control the initialization of the printed circuit board under test. This can be accomplished by socketing the PROM at address XXXX-FFFF, or by providing access (via a control point) so that the test system can deselect it and emulate locations FFFE and FFFF.

Output test points, which are important for synchronization of data input and output, include VMA (valid memory address) and R/(not)W (read write status).

The following figure summarizes the testability rules for the 6800 microprocessor (figure 9-3).



```
A) Provide control of Ø1 and Ø2 clock inputs (see Figure
   4-24).

B) Provide input control points for:
      RESET*
      NMI*
      DBE
      TSC
      HALT*

C) Provide output test points for:
      R/W*
      VMA
      BA

D) Provides for address and data bus access.
```

Figure 9-3. 6800 Testability Rules Summary

The 6802 (not shown) adds an on-chip clock and RAM to the 6800.

The address bus cannot be floated with this device, even though /HALT will float the data bus. Proper design for testability (which will also allow the system design to address the address bus) is to buffer AO-A11 with drivers that have a tri-state control.

Another key consideration is control of the RE line (on-chip RAM enable), so that the ATE system can check out the microprocessor functions (from the same memory locations as with the 6800), and then perform software initialization of the on- chip RAM).

An advantage to be gained is that after a write/verify with read sequence, the sequence can be used to let the CPU free run to test other portions of its functions, thus reducing test program stimulus generation effort.

9.4.1.2 The 8085A Microprocessor Family (8-Bit Microprocessor). The 8085 microprocessor has several distinct differences from the obsoleted 8080A. Among these differences are:

1. The +12 and -5 volt power supply requirements are eliminated.

2. The 8085 multiplexes its low order address lines (A0-A7) with the data bus (D0-D7). The pins are labeled ADO-AD7. (See figure 9-4 for pin-out).

3. An on-chip clock, which may be driven by a single clock input, twice the processor operating frequency, has been provided.

From a testing and testability standpoint, items 2 and 3 above represent a mixed blessing. While the multiplexing of address and data lines complicates the ATE programming task, the ability to drive the on-chip clock from the ATE, as long as testability is considered, is a distinct advantage.

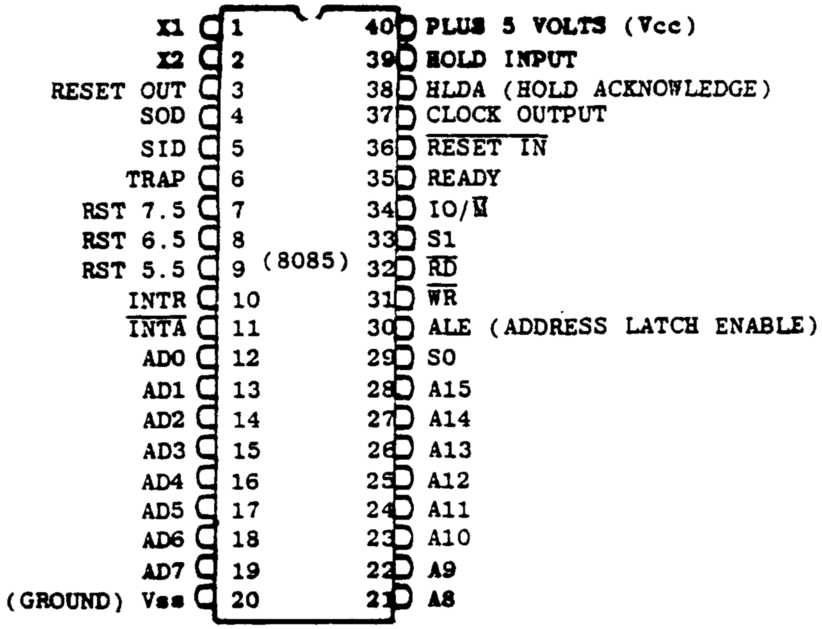


Figure 9-4. 8085 Block Diagram (DIP)

To design in testability, the first step is to provide for clock control. The 8085A on-chip clock can be derived in two ways, as illustrated in figure 9-5.

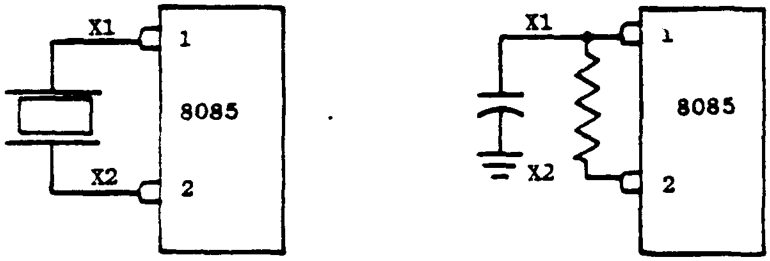


Figure 9-5. 8085 Clock Derivations

If the clock is generated in either of these ways, the test system will not have control of the clock lines. For testing purposes, the best method of providing clock control is either a jumper or a switch to allow the X1 input to be driven as if it were in the slave mode. One example of this is illustrated in figure 9-6.

Just as important as clock control is access to control and observability points. Edge connector access is best, followed by a special test connector, IC clips or a bed of nails fixture.

With the 8085A, the control lines needed include:

1. READY
2. HOLD
3. TRAP
4. /RESET IN

Access to these lines provides for initialization of the microprocessor, tri-state of address and data lines to facilitate a partitioned test programming approach, interleaving test program data with hold signal functions on I/O rate ATE systems and control of the non-maskable interrupt (TRAP). The test systems should have control of the TRAP line to prevent a condition on the Unit Under Test (UUT) from causing response to an interrupt when there may be uninitialized data internal to the 8085A. Should an interrupt be serviced when the processor is not totally initialized, unknown or "X" states will be propagated throughout the UUT. This makes debugging a microprocessor based UUT much more difficult.

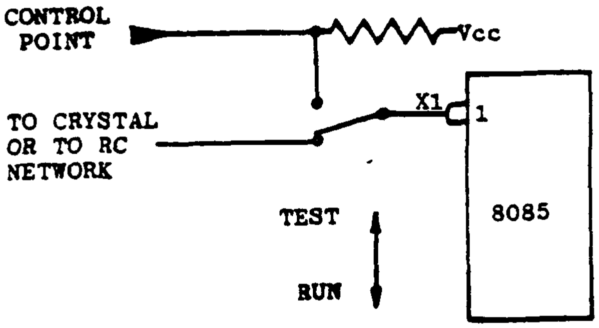


Figure 9-6. Example of Clock Control

The observability points that should be available to the ATE system include:

1. The address latch enable line (ALE).

2. The S0 and S1 BUS state indicator lines. These status signals can be used by the tester (or tester interface) to decode the type of operation being performed at a given time.

3. The /RD, /WD and IO/(not)M lines. These signals can be used to determine proper clocking, strobing, and data availability to and from the unit under test.

Some of the above lines go into the tri-state condition in response to control signals. All lines that can be tri-state should have pull-up resistors attached (figure 9-7).

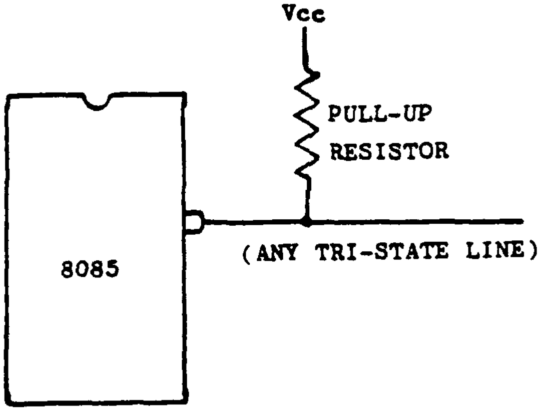


Figure 9-7. Pull-Ups on Tri-state Outputs

9.4.1.3 The Z80 Microprocessor Family. The Z80 requires only a single +5V power source and a single clock input. All 8085 instructions can be executed by the Z80 plus some additional instructions.

Z80 control and test point requirements are listed below. As with all of the processors discussed thus far, provision for driving the clock input externally from the ATE system is an extremely important requirement.

Control Points	Test Points
/RESET	/RD
/BUSRQ	/WR
/WAIT	/IORQ
/NMI	/M1

Most of the discussion of the 8085A family also applies to the Z80 device.

Access to /RESET is required to isolate the CPU for a partitioned test and to reset the program counter, IV, and R registers to zero. Interrupts are disabled after a reset operation, except for non-maskable interrupts via /NMI. Design criteria should ensure that the test system can prevent or control /NMI so that no non-maskable interrupts occur or are serviced prior to software initialization.

Access to /WAIT allows an I/O rate test system or in-circuit test system to be used to test the Z80. The /BUSRQ allows tri-stating of the address and data buses for access to other devices without resetting the Z80 (or the entire printed circuit board under test).

The output test points (/RD, /WR, and /IORQ) are needed to allow the interface to decode proper tester clock and strobe times (in conjunction with the clock input signal to the Z80), so that only valid data is driven in to the device, and output data is valid when compared.

To test the interrupt circuit, it is often desirable to have a signal available called "interrupt acknowledge". While there is no single Z80 pin with this function, the function can be derived with the circuit of figure 9-8.

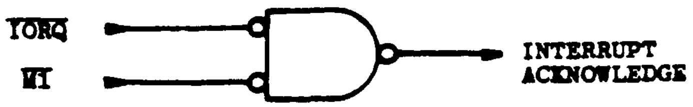


Figure 9-8. Interrupt Acknowledge

Many of the 8085A support devices can be used in Z80 systems. Two devices, the parallel I/O interface (PIO) and the counter/timer circuit (CTC), are unique to Z80 designs.

The Z80 PIO is a 40 pin-dip, requiring a single +5V power supply and a single clock input. Since in most systems this clock input will be driven from the same clock as the Z80, separate access is not required (assuming that the guideline for Z80 clock control has been followed).

Important control points for this device include:

1. /CE, the chip enable line. Access to this line is required to tri-state its outputs for testing other devices on the bus.

2. Access to B/(not)A (port select) and C/(not)D (control /data select) lines. These lines provides a means of a thorough device test without needing to use the Z80 CPU to generate stimulus test vectors.

Important test points for this device include:

1. The A RDY and B RDY (the port A and port B READY) lines provide information to the ATE for clocking and strobing data in and out of the PIO.

2. /INT, the interrupt request output. This output goes low when an interrupt is to be output to the Z80 CPU. This output is the CMOS equivalent (open drain) to a TTL open collector line, and should therefore have a pull-up resistor provided so that it will not float in the unknown or error region (e.g., above 0.80V and below 2.4V). The PIO can be reset by inputting the following signals:

/MI	/IORQ	/RD
0	1	1

In order to test the Z80 PIO, it must first be set up with a control code. The format for appropriate control codes is shown in figure 9-9.

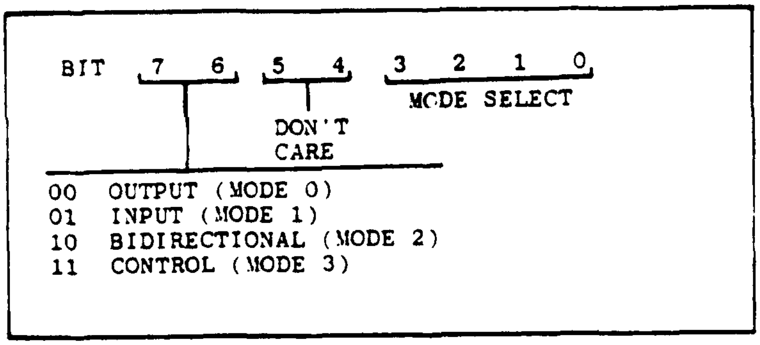


Figure 9-9. Z80 Setup Control Code

The Z80 clock/timer circuit (CTC) is a programmable device with four sets of timing logic, which are separately programmable as internal timers or external event counters.

Test and control points for this device are similar to those described for the PIO and are summarized below.

Control Points	Test Points
/CE	* /INT
/RESET	

(*open drain)

Testing this device requires software initialization (if done by the processor) or its equivalent via stimulus from the ATE system. The procedure is:

1. Output an interrupt vector when initializing the CTC

2. Output control codes to each of the four sections of the device.

The interrupt vector specifies which channel will receive the control code. An appropriate sequence for channel 0 as a counter via the Z80 CPU is shown in figure 9-10.

```
LD    A, 2C
LD    1, A
IM    2
LD    A, 40
OUT   (0B8), A    (INTERRUPT VECTOR)
LD    A, 0C5
OUT   (0B8), A    (CONTROL CODE)
LD    A, DATA     (DATA=INITIAL COUNT)
OUT   (0B8), A    (START CHANNEL 0)
```

Figure 9-10. Sample Z80 Interrupt Vector Sequence

9.4.2 16-BIT (CISC) Microprocessor. The following paragraphs give examples of testability of 16-bit CISC microprocessors: the 8086 (8088), the Z8000, and the 68000 families.

9.4.2.1 The 8086 Microprocessor Family.

The 8086/88 architecture received its most popularity when it was chosen for the original IBM-PC. The 8088 family member is identical to the 8086 except that it only has an 8-bit data bus. It was also used in later models of the IBM PC. In 1987 the 8086 family architecture and its clones had gained 80% of the 16-bit and above microprocessor market. Both the 8086/88 run with the 8087 coprocessor.

Intel's 80186/88 high performance 16-bit processor never gained much popularity (both also use the 8087 coprocessor).

(Intel's 80286 is the present microcomputer work horse. It is an advanced 16-bit microprocessor of which Intel shipped 4 million units in 1987. It is used in the IBM-PC AT and all its clones and second sourced by a half a dozen companies). (See section 9.4.2.3).

The 8086 has changes and additions compared to its predecessor, the 8085A, including the following:

1. The 8086, having been designed to work in both large and small configurations, has been equipped with a number of output pins which may have different signals depending on the state of pin 33 (MN/(not)MX). These different signals, depending upon the selection of "minimum system" or "maximum system" usage, are listed with the pin-out of the device in Figure 9-11.

2. The CPU has been divided into two halves, called the execution unit (EU) and the bus interface unit (BIU). These two sections operate asynchronously.

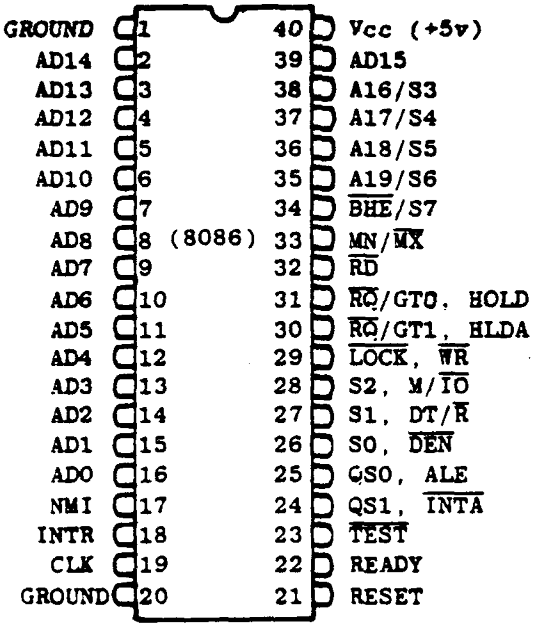


Figure 9-11. 8086 Block Diagram (DIP)

3. The 8086 can have its own local memory and can also share common system memory in multiple processor designs. This means that particular care must be taken in system (board) design to ensure control of all memory elements.

The 8086 uses a multiplexed address/data bus, which can complicate both the test interfacing and the test programming from a timing and handshake standpoint. It is one of the few processor designs, however, that incorporates at least minimal design for testability in the form of pin 23 (/TEST).

The /TEST pin can be used for a number of purposes. Among them are:

1. The wait state for the execution unit can be initiated via software (as opposed to the hardware wait state, which is forced by the READY input) to cause a continuous sequence of idle clock periods. The bus interface unit is still active, however, and can be used to fill up the instruction queue via memory read bus cycles, thus allowing software initialization of the EU. This wait state is terminated by applying a logic 0 to /TEST.

   To make use of this capability from a testability standpoint, it is imperative that the test engineer be able to initiate a program-induced wait state immediately following the reset operation. The design can allow this access in a number of ways, including socketing the ROM devices, or providing chip deselect control. This way the test programmer can use the ATE stimulus patterns to initiate the programmed wait state and achieve software initialization on the board.

2. The wait state can be used to synchronize two or more processors in a multiple processor system, or to synchronize the processor with the ATE system. Thus the execution unit can be loaded (via the BIU) with simple subroutines, whose execution can be controlled via the /TEST pin. Execution will begin when /TEST is driven low.

As with all microprocessors, the reset operation should be performed first. The 8086 has an asynchronous RESET input, which can be driven high at any time. The logic 1 state must remain high for at least four clock cycles. The reset operation begins when the RESET pin is driven to logic 0. The reset operation takes approximately ten clock periods for completion and must be synchronous with the clock when RESET is driven low.

An example of an 8086 testing strategy might be to reset the device, input a wait instruction from location FFFFO (e.g., from the ATE system). Then exercise each portion of the device with a simple program such as:

1. Drive /TEST to logic 1

2. Input the first test
   wait
   instruction, data
   instruction, data
   (tests the program counter)

3. Input the next test
   wait
   instruction, data
   instruction, data
   (tests the ALU).

The ATE system can then cause each small subroutine test to execute by pulsing TEST to a logic 0 and checking the results when the EU has entered the next wait state.

The control points needed for testability for the 8086 include:

- NMI, the non-maskable interrupt request line
- INTR, the interrupt request line (maskable)
- CLK, the system clock, derived from the ATE or more commonly from an 8284 clock generator/driver
- /TEST, the test input line
- RESET, the device reset line
- READY, the wait state request line.

Observability points needed, in addition to the address/data bus lines, include:

- (not)BHE/S7, the high order BYTE/Status output
- /RD, the read control line (to allow handshake with the ATE and recognition of proper clock and strobe times)
- Pins 24 through 29, the multipurpose outputs. Their use by the ATE system will depend on the state of the MN/(not)MX line.

Most of these observability points can be tri-stated to allow testing of other devices on the board using the previously described partitioning approach.

The 8086 derives its clocks input from the 8284 clock generator/driver. The pin- out for this device is shown in figure 9-12.

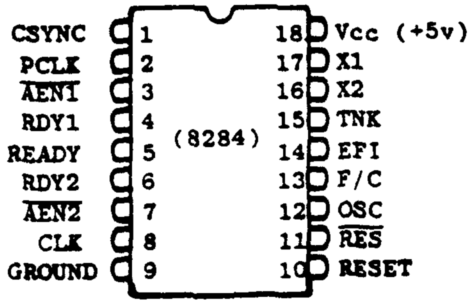


Figure 9-12. 8284 Block Diagram (DIP)

The control points needed for this device include:

- CSYNC, the clock synchronization line
- EFI, the external clock input
- F/C, the clock source select line
- /RES, the RESET input (which is later transformed to the 8086 reset output at pin 10, reset)

- RDY1 and RDY2, the wait state inputs
- /AEN1 and /AEN2, the address enable qualifiers for RDY1 and RDY2.

The input at EFI must be three times the frequency of the 8086 clock period. Provision must be made on the board under test to disconnect the tank and/or crystal circuits in order for the ATE system to control the 8284 frequency.

Since the 8086 is designed for multiple processor applications, it is important that all clocks be derived from a single source and not from multiple asynchronous 8284 devices.

A simple circuit for providing clock and synchronization of resets in a multi-processor board is shown in figure 9-13.

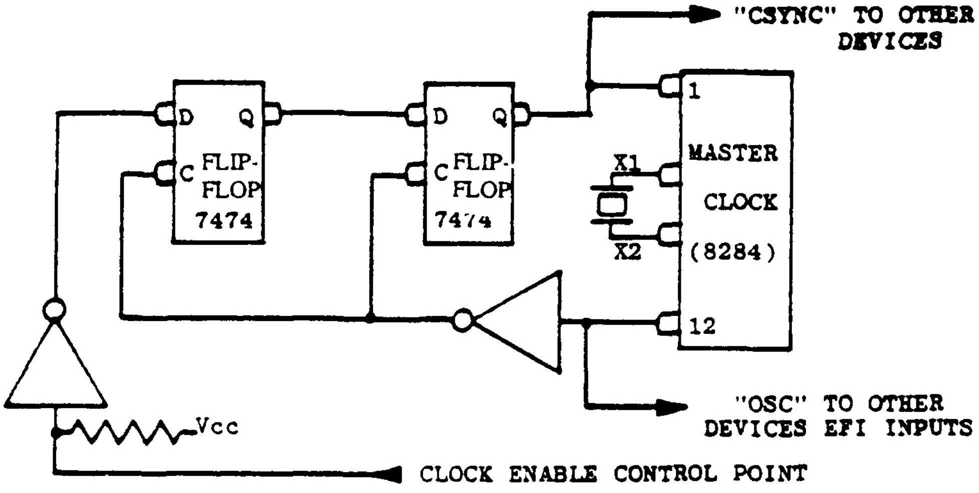


Figure 9-13. Sample Clock/Sync Circuit

Completion of a minimum 8086 system requires the use of the 8288 bus controller. The pin-out for this device is shown in figure 9-14.

All of the 8288 control outputs normally connected to the system bus can be tri-stated, as long as control of the IOB (mode control) line is possible. If the system design uses the 8288 in the I/O bus mode, the IOB pin should not be tied directly to Vcc. It should be tied through a pull-up resistor, to allow the test system to isolate the 8288 from the bus.

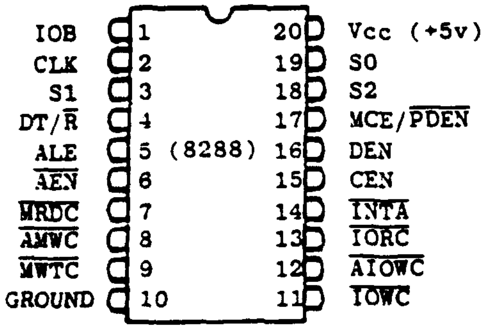


Figure 9-14. 8288 Block Diagram (DIP)

When a microprocessor board is to be tested running at speed, the 8288 will provide an output, /AMWC (advanced memory write control), which is one clock pulse in advance of the normal 8086 write signal. This will allow setup of ATE response data in advance of the 8086's output, thus simplifying the strobing requirements.

Other input control points where access is desirable include:

- CLK, the clock input
- /AEN, the bus priority enable/control line
- CEN, the control enable line.

The proper control input states for isolating the 8288 from the rest of the system are:

/AEN	CEN	IOB
1	0	0

Two other devices that support the 8086 are the 8282 8-bit input/output port and the 8286 8-bit bidirectional bus transceiver. For these devices, access is needed to the /OE and STB pins (8282) and to the /OE and T pins (8286).

A great many other support devices are used with the 8086. For the most part, the guidelines for these devices follow those for previously described devices. One device that presents special considerations is the 8202 dynamic RAM controller, which is used with the 2104A, 2117, and 2118 dynamic memories (with the 8085 as well as the 8086). The pin-out for the 8202 is shown in figure 9-15.

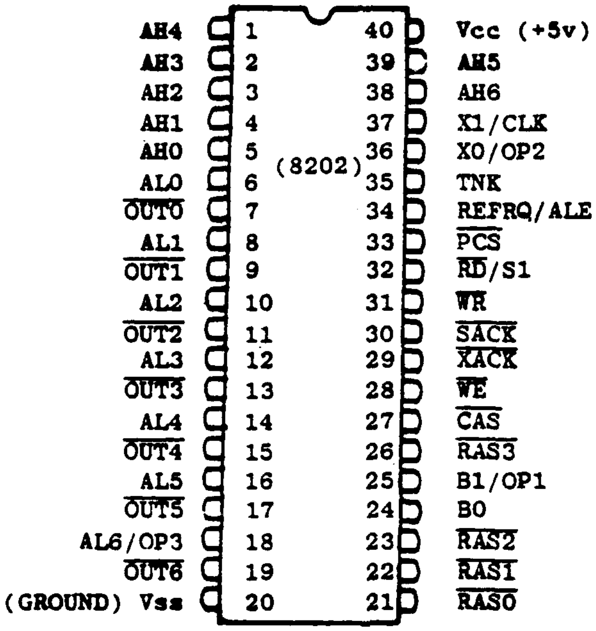


Figure 9-15. 8202 Block Diagram (DIP)

Because this device can run at a very high rate, control point access to the clock to allow the 8202 to be driven externally is very important. This can be accomplished by providing a means to pull pin 36 (XO/OP2) high to +12 volts via a 1K ohm resistor. The external clock must then have access to pin 37 (X1/CLK), which is designed for TTL levels.

Output test points needed include /WE, /CAS and /RASO through /RAS3. Input control point access should include RD/S1, /WR, and /PCS. Access to /RD/S1 and /WR allows initiation of a test cycle, which will reset the refresh counter to zero and force the 8202 to execute a write cycle.

9.4.2.2 80186. The 16-bit 80186 CPU includes two high-speed direct memory access channels, timers, and I/O control on one chip. It is twice as fast as the 8086 and addresses more memory (direct memory address of 1 Mbyte). With its numerical coprocessor, the 8087, it offers direct execution of trigonometric, exponential, and logarithmic instructions. It has seen only limited use as a controller chip.

9.4.2.3 80286. The 16-bit 80286 processor executes 6 times faster than the 8086. The processor has a large memory capacity of 16 Mbytes and using virtual memory each task can reach 1 gigabyte (Gbyte). Memory management as well as protection is integrated into the microprocessor. Using the 80287, high-performance numerical processing can be done. Other than for Personal Computers (PCs), the 80286 has had little success on the general market.

9.4.2.4 The 68000 Processor Family. The 68000 processor family owes much of its popularity to the Apple/MACs. The family consists of the 68000, 68008 (8 BIT data bus), 68010, 68012, 68020 and the 68030 (68040 due out late 1990 and 68050 due in 1992).

The 68000 is being second sourced by Rockwell, Hitachi, Mostek, Signetics/Phillips and Thompson/Sgs. (No one is second sourcing 68020 or 68030 so far.). See figure 9-16.

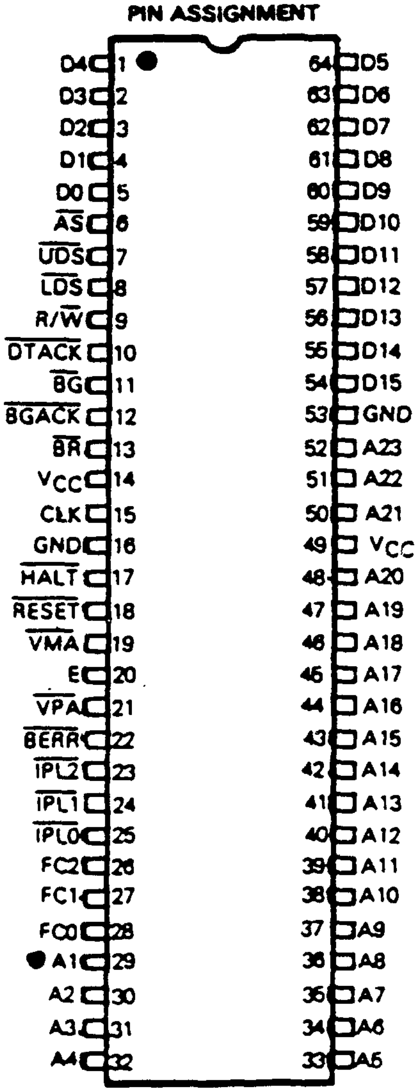


Figure 9-16. 68000 Block Diagram (DIP)

The M68000 family (all internal registers 32 bits wide) has a 16 bit wide data bus. Memory addresses up to 16 Mbytes are reached by the 24-bit program counter. The processor (in a 64-pin DIP) provides a 16-bit data bus and a 23-bit address bus, plus control and power pins. The 24th bit of the address bus is a combination (by external gating) of the address strobe with two data lines.

A +5V power supply and two grounds are required. A single-phase TTL-level clock (up to 8 MHz) provides timing. Existing MC6800 family support chips can be used with this family, with a few exceptions.

In 1989 the 68000 and its successors were at the heart of more than 60% of all computer systems priced from $12,000 to $300,000.

With its built-in bus arbitration logic and prefetch circuitry, the 68000 family has become a favorite for designers with multi-processing and multi-tasking needs.

The clocks to these processors should always be kept running while power is applied.

Control should be provided for the following signals:

1. /RESET This bidirectional signal is used to initialize the program counter and it should be brought to an edge connector.

2. CLK This signal should be controlled using standard clock control method described in section 7.

3. /HALT This bidirectional signal needs a separate pull-up resister and should be brought to an edge connector.

4. /VPA The Valid Peripheral Address signal needs a separate pull-up resistor and should be brought to an edge connector. It provides critical control for asynchronous testing.

5. /DTACK The Data Transfer ACKnowledge (see /VPA).

6. /BR The Bus Request signal is wired-ORed with all other present or potential bus master signals. A test point should be used for access.

7. /BGACK The Bus Grant ACKnowledge signal should also have a test point.

8. /IPL (0:2) These lines indicate priority levels of devices requesting interrupts. See /VPA.

9. DATABUS (D0:D7) The bidirectional signals control the data presented to the CPU. This bus should be buffered.

The following observability points should be provided:

1. /AS The Address Strobe signal shows that a valid address is on the bus line. A test point should be provided to this signal.

2. /LDS The Lower Data Strobe signal should have a test point.

3. /UDS The Upper Data Strobe signal shoulu nave a test point.

4. ADDRESS BUS (AD1:AD23) These lines provide the addresses for bus operations for all cycles, except interrupt cycles.

   At an interrupt cycle A1, A2, and A3, provide this interrupt level being serviced (A4:A23 are set HIGH).

   These signals should be brought to edge connector pins. Also, individual pull-up resistors should be used.

5. /VMA The Vector Memory Address signal monitors/controls CPU activity and should have a test point.

6. E Enable signal /(see VMA).

7. R/(not)W This signal defines the data bus transfer for either a read or a write cycle. It should be provided with a test point.

8. FC0:FC2 The three Function Code Outputs provide information on the currently executing state and cycle types. Three separate test points should be provided.

9. /BG The Bus Grant signal should be provided with a test point.

9.4.2.4.1 The 68008 Processor. This device is 100% software compatible with the 6800, the 68000, and the 68010. It includes a 20 bit address bus, an 8 bit tri-stateable data bus, and needs only a 5 volt supply. All of this is packaged in a 48 pin DIP.

The control and observability lines are practically identicai ιo the 68000.

9.4.2.5 The Z8000 Microprocessor Family. The Z8000 family of processors described in this section includes the Z8001 and Z8002 CPUs, the Z8010 MMU (memory management unit) and the Z8034 UPC (universal peripheral controller). The Z8001 is a 48-pin dip, while the Z8002 is a 40-pin package. The primary difference between the two devices is that the Z8001 has the extra pins to handle additional external memory segments. For testability purposes, this section will use the Z8002 (pin-out shown in figure-17).

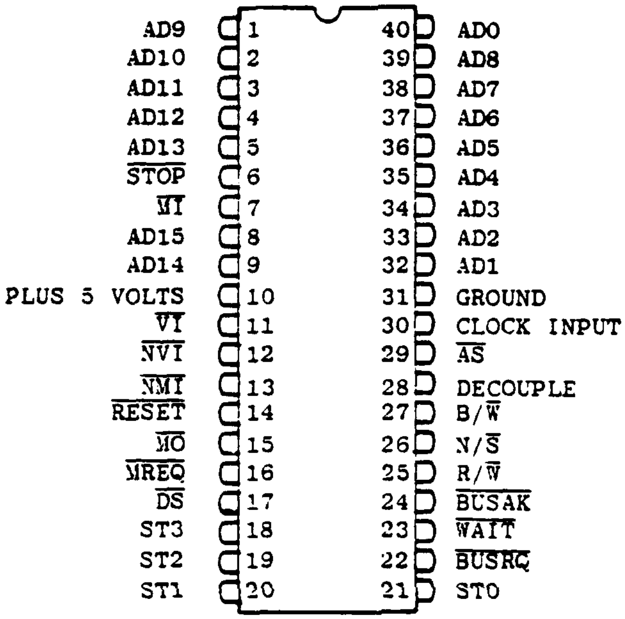


Figure 9-17. Z8002 Block Diagram (DIP)

The Z8000 CPUs (similar to 8086A family) multiplex the address and data lines (adding another dimension to the complexity of testability). Many of the comments applicable to the 8086 are also applicable to the Z8000 family.

The Z8002 requires a single clock input from the ATE for control.

All but two of the output lines from the Z8002 can be tri-stated; needing pull-up resisters on these lines.

Output test points needed (in addition to the standard observability rules) include.

- R/(not)W, the read/(not)write select lines.

- ST0-ST3, the machine cycle status lines.

- /AS, the address strobe line. This line is low when an address is being output by the processor and always occurs at clock cycle T1.

- /DS, the data strobe line. This line is low when data is being inputted or output to and from the processor and always occurs at clock cycle T3.

- /MREQ, the memory request line.

Access to these lines assists the test engineer in clocking and strobing data to and from the test system and the UUT.

The address and data strobe lines provide the necessary information about the state of the bus so that the proper operation can be performed at each test step.

Input control points include:

- /RESET, (the reset input to the device). A low at this input will initialize the processor and tri-state all outputs (except /BUSAK and MO (not)). Access to /RESET should be provided.
- /BURSQ, (bus request input). Access allows tri-stating of the address/data bus, without resetting the CPU or unit under test. This is equivalent to the hold state in other processors.
- /NMI, (non-maskable interrupt.) Either provide access or make provisions not to allow occurrence of a non-maskable interrupt before ATE initialization.
- /WAIT, (wait state input.) This function allows the CPU to place idle clock periods into machine cycles so UUT can be tested at less than full clock speed.
- /STOP, (stop input.) This allows processor control on an instruction-by-instruction basis (as opposed to cycle by cycle with the WAIT (not) line), providing a function similar to one implemented for the 8048 family.

The Z8010 MMU is used with the Z8001 where very large memory requirements exist. The pin-out is shown in figure 9-18.

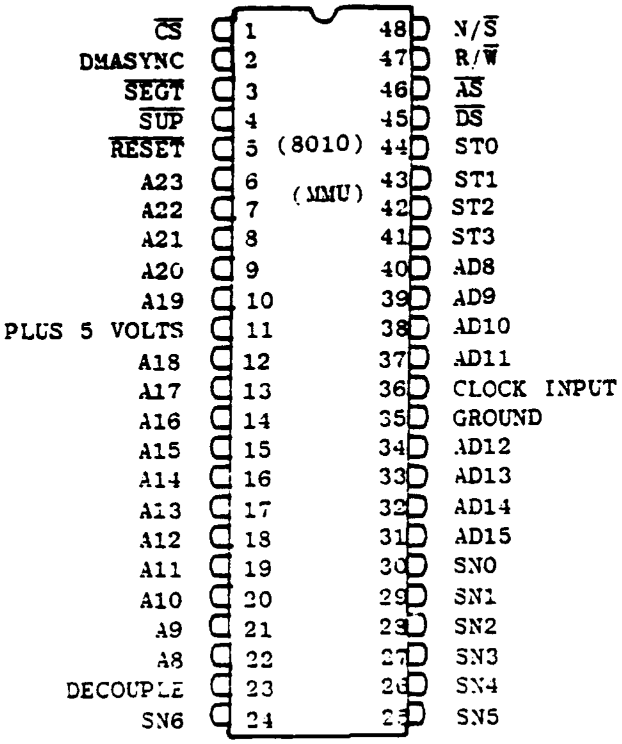


Figure 9-18. Z8010 MMU Pin-Out

The main consideration is control point access to /CS, the chip select input, which allows isolation of the device from others on the UUT. The pin-out for the Z8034 is shown in figure 9-19.

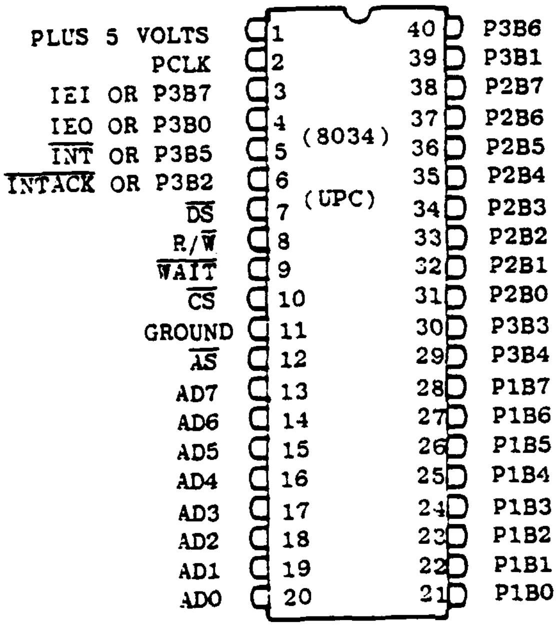


Figure 9-19. Z8084 Pin-Out

This microcomputer operates as a slave to the Z8000, including 2,048 bytes of on-chip ROM. The ROM code should allow immediate access for control by the ATE. The chip select line (/CS) needs to be controllable by the ATE system.

9.4.3 32-Bit (CISC) Microprocessor. In the industry it has become a fairly straightforward process to go from 8 to 16 to 32 bit microprocessors. This development has come about from an increased industry need of extended addressing capability, more precision and a larger bandwidth.

The 32-bit (CISC) microprocessor market really started to take off in 1987 when world sales grew 230% to approximately 300 million dollars. In 1988 the market more than doubled by the demand to support multi-user and multi-tasking applications.

The 32-bit microprocessors will probably remain the standard workhorses well into the 90s.

The top companies in terms of market share for the 32-bit (CISC) processors are in order of business: Intel, Motorola, Intergraph, and INMOS.

In this section we will look at the testability of three of the most popular 32-bit (CISC) microprocessors on the market today: the Intel 80386, the Motorola 68030, and the Intergraph "CLIPPER" C300.

9.4.3.1 The 80386 32-Bit (CISC) Microprocessor. This chip is compatible with the 8086, 80186, and 80286 families. It includes address translation registers and a 32-bit address bus for up to 4 Giga bytes of physical memory and 64 Tera bytes of virtual memory. It runs DOS Windows, OS/2, and UNIX, etc.

An 80386SX chip is equivalent to the internal workings of the 80386, but has only a 24-bit address bus and a 16 pin data bus making for a smaller and cheaper chip.

The 80386, as analysts see it, will remain the dominant 32-bit microprocessor for the early nineties. It is packaged in a 132-lead ceramic PGA and can run at 33 MHz top speed. (See figure 9-20).

Designing a 32-bit microprocessor circuit for testability is a very complex task due to the complexity of the chip itself. Before starting the task, a thorough understanding of the accompanying microprocessor literature and I/O lines is necessary.

(It should be noted that no second source exists for this chip or is planned in the immediate future although AMD is trying to MARKET a similar chip).

Many of the rules and techniques for Testability Design of 16 BIT microprocessors apply to 32 BIT microprocessors in general.

Access to all address lines (A2-A31) and all data lines (DO to D31) and the four BYTE enable lines /BE0 - /BE3 is a must, as well as access to the control and visibility points shown later.

9.4.3.1.1 80386 BUS Interface. The 80386 bus interface consists of four bus groupings, the 32-bit data bus, the address bus consisting of 30 address bits and 4 byte-enable lines (/BE0-/BE3), 5 status lines, and a 12-bit control bus.

9.4.3.1.2 80386 Data Bus. The data bus, (D0-D31) is bidirectional and can be allocated dynamically to transfer 32, 24, 16 or 8 bits of data as a unit. The address bus includes A2-A31 and four byte-enable lines, /BE0-/BE3. The 30-bit address lines are used to select one of four billion one-byte locations. This is equivalent to a 32-bit memory address that can access 2^{32} or four billion byte locations.

9.4.3.1.3 80386 Status Output Lines. The five status output lines are Address Status /(ADS), Write/Read (W/R), Memory I/O (M/(not)IO), Data/Control (D/(not)C), and /LOCK. The /ADS output is active low and indicates that the addresses present on the address bus are valid. Memory//(I/O) or M/(not)IO indicates a memory transfer if high and an I/O transfer if low. A high on Data/Control (D/(not)C) indicates data transfer involving memory, while a low indicates an instruction transfer involving memory. If /LOCK is low, the bus is locked. This means that another bus master cannot use the local 80386 bus and ensures read-modify-write operations without interruption.

9.4.3.1.4 80386 Control Bus. The control bus consists 11 inputs and 1 output. The inputs are /READY, Next Address /(NA). Bus Size 16 /(BS16), CLK2, RESET, HOLD, Maskable Interrupt (INTR), Non-maskable Interrupt (NMI), /BUSY, /ERROR, and Coprocessor Request (PEREQ). The output is Hold Acknowledge (HLDA). READY is active low and, when active, terminates the current bus cycle. When a high input is placed on /READY, a wait state is added to the bus cycle. /READY is sampled in each additional wait state and adds another wait state each time until /READY is sampled low.

The 80287 or 80387 numeric coprocessors provide numeric processing capabilities to the 80386 such as high-precision integer and floating-point calculations. The 80387 performs 32-bit data transfers while the 80287 performs 16-bit transfers. The coprocessor is selected through I/O addresses from the 80386 through the execution of coprocessor instructions. The active low ERROR input to the 80386 indicates an error (not masked by the coprocessor control register) has occurred after a mathematical instruction is execution by the coprocessor.

9.4.3.1.5 Bus Timing. The 80386 bus cycle has a minimum of two states, T1 and T2. (The clock signals CLK2 and CLK). CLK2 is an externally applied synchronization signal for the 80386 divided by two internally by the microprocessor to produce the CLK signal. Each state consists of two CLK2 phases.

9.4.3.1.6 Testability, Self-Test;. (taken from Intel 1989 data books with permission from Intel). The self-test checks the function of the Control ROM and most of the non-random logic. Approximately half of the 386 Microprocessor can be tested during self-test.

Self-test is initiated by the RESET pin transition from HIGH to LOW, and the BUSY pin is low. The self-test takes about 2^{19} clocks, or approximately 33 milliseconds with a 16 MHz 386 Microprocessor. Upon completion of self-test the processor performs reset and begins normal operation. The part has successfully passed self-test if the contents of the EAX register are zero (0), if not then the self-test has detected a microprocessor flaw.

Additionally, the 80386 has some provision to test the transition Look-aside Buffer (TLB). The TLB is a 32-entry cache designed to automatically track the most commonly used Page Table Entries when running the on-chip memory paging option. The 80386 has two test registers (TR6 and TR7) set aside as a testability feature to enable entries into the TLB and to perform TLB look-ups.

* NOTE: Information for paragraph 9.4.3.1.6 was taken with the kind permission from the Intel Corporation, Copyright/Intel Corporation data book, 1990. Refer to same book for more detailed info which is out of scope of this handbook.

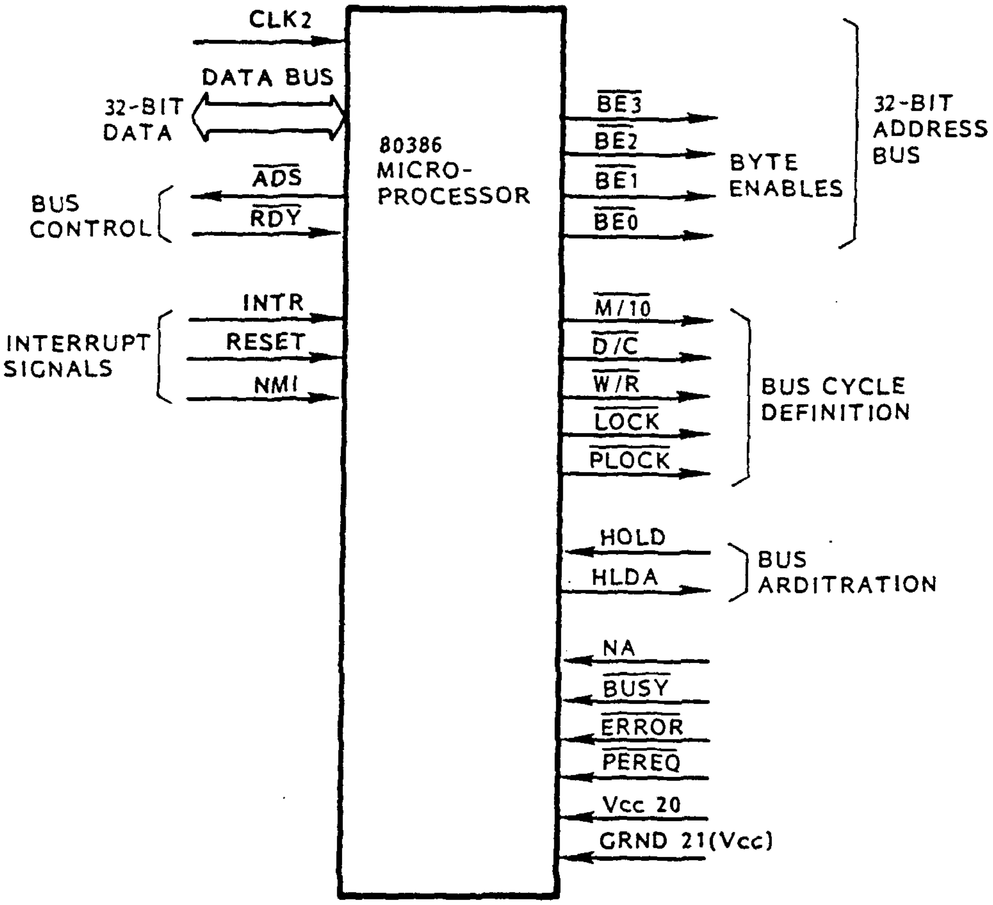


Figure 9-20. 80386 Block Diagram

1. Control points include:

   The 11 inputs: Ready, /NA, /BS16, CLK2, Reset, HOLD, INTR, NMI, /BUSY, /ERROR and PEREQ.

2. Visibility or test points include:

   The control bus output: HLDA, the 5 status output lines /ADS, W/(not)R, M//IO, D/(not)C and /LOCK.

9.4.3.2 80486 Microprocessor. The 80486 is a faster version of the 80386 also running at 33 MHz but including not only an 80386 CPU but a 80387 math coprocessor, a 82385 code controller, an 8 Kbyte combined cache and data code, and a paging and memory management unit all on the same chip (see figure 9-21).

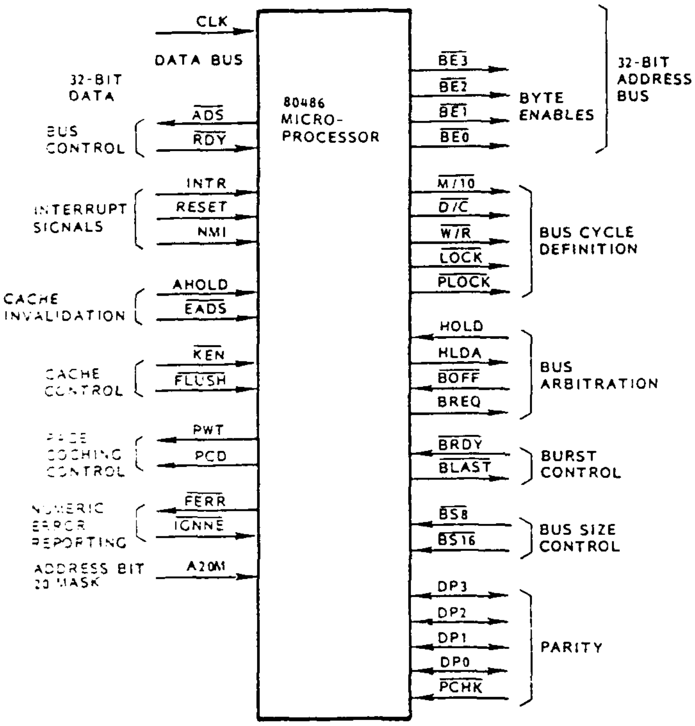


Figure 9-21. 80486 Block Diagram

The 80486 runs UNIX and is a match for low end RISC-based processors. The 80486 block diagram shows the 80486 pin functions. The 32-bit address bus is implemented as 30 address bits, plus four byte enables that encode the two least- significant address bits and the transfer width. Many of the control signals, are similar to their 80386 counterparts (see paragraph 9.4.3.1.6). The 80386 provides dynamic bus sizing for 16-bit devices via the /BS16 (bus size 16 bits) signal; the 80486 adds a /BS8 (bus size 8 bits) signal to support byte-wide devices. The rest of the signals represent new features.

The 80486 implements a single-phase clock, so the internal and external clocks have the same frequency. This technique, first tested by Intel with the 80860, simplifies an ATE interface as well as system design and make it easier to meet FCC emissions standards.

9.4.3.2.1 Testability. The 80486 is a very complex chip whose design notes need to be carefully studied before testability is implemented. Many of the 80386 techniques can be applied as can the earlier 16-bit microprocessor techniques.

Testing an 80486 can be divided into two classes:

1. Built-in Self Test (BIST): Tests non-random logic, control ROM (CROM) cache memory (on-chip) and Translation Look aside Buffer (TLB).

2. External Testing: Tests run on the TLB and on-chip cache memory. The '486 chip also includes a TEST MODE which tri-states all outputs.

Note: Section 9.4.3.2.1 was taken with the kind permission of Intel from the Intel Microprocessors (1990) Data Book.

9.4.3.2.2 Recommended Testability Access.

1. Control lines include: CLK, /RDY, INTR, RESET, NMI, AHOLD, /EADS, /KEN, /FLUSH, /IGNNE, /A2OM, HOLD, /BOFF, /BRDY, /BS8, /BS16.

2. Visibility or test points include: /ADS, PWT, PCD, /FERR, /BE0 to /BE3, M/(not)IO, D/(not)C, W/(not)R, /LOCK, /PLOCK, HLDA, BREQ, /BLAST, /PCHK.

For further infonnation see the latest Intel Microprocessor Data Books.

9.4.3.3 The 68030 32-Bit (CISC) Microprocessor. This chip is the latest available 32-bit microprocessor from Motorola. It includes a 68020, data cache and a subset of the 68851 MMU all on one chip. It will run 30 to 50 MHz. This chip used CMOS technology and is packaged in a 128 pin grid array. See figure 9-22.

Like the 68020, the 68030 is object code compatible with the 68000, 68008, 68010, and 68012 microprocessors.

Again many of the testability ideas of the earlier 16-bit processors hold here.

Accessibility to all address lines A0-A31, data lines D0-D31 is a must:

1. Control lines include: /DSACK0, /DSACK1, /CIIN, /CBACK, IPL0-IPL2, /AVEC, /BR, /BGACK, /RESET, /HALT, /BERR, /STERM, /CDIS, /MMUDIS, CLK IN, Vcc, GND.

2. Visibility or test points include: FCO, FC2, SIZ0, SIZ1, /OCS, /ECS, R/(not)W, /RMC, /AS, /DS, /DBEN, /CIOUT, /CBREQ, /IPEND, /BG.

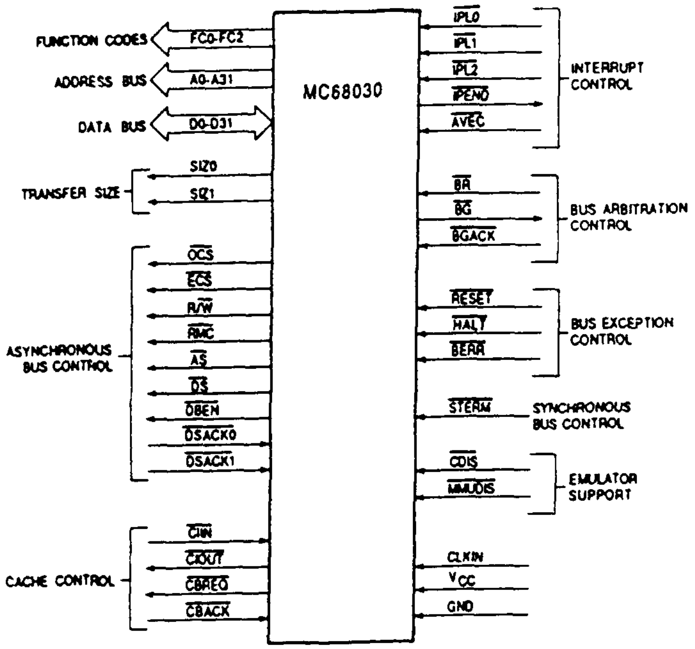


Figure 9-22. MC68030 Functional Signal Groups

9.4.3.4 The Intergraph CLIPPER C300. This is a second generation 32-bit (CISC) microprocessor. The CLIPPER was originally built by Fairchild which has since been bought by Intergraph.

It is actually a module consisting of 3 ICs; a CPU chip, and two CACHE-MMU chips (called CAMMUs). One CAMMU is instruction dedicated, the other is for data only. These CAMMUs are each connected to the CPU with their own dedicated bus. The CPU chip also contains a floating-point Unit (FPU) on board. (See figure 9.23).

The CLIPPER C300 chip set boast impressive statistics:

1. It is as fast as a VAX8800 (running VMS) in both integer and floating point performance.

2. It can run up to 3 to 5 times faster than the 25 MHz Motorola 68020/68881 chip set.

3. It can achieve 15 VAX MIPS.

See figures 9-23, 9-24, 9-25 and 9-26.

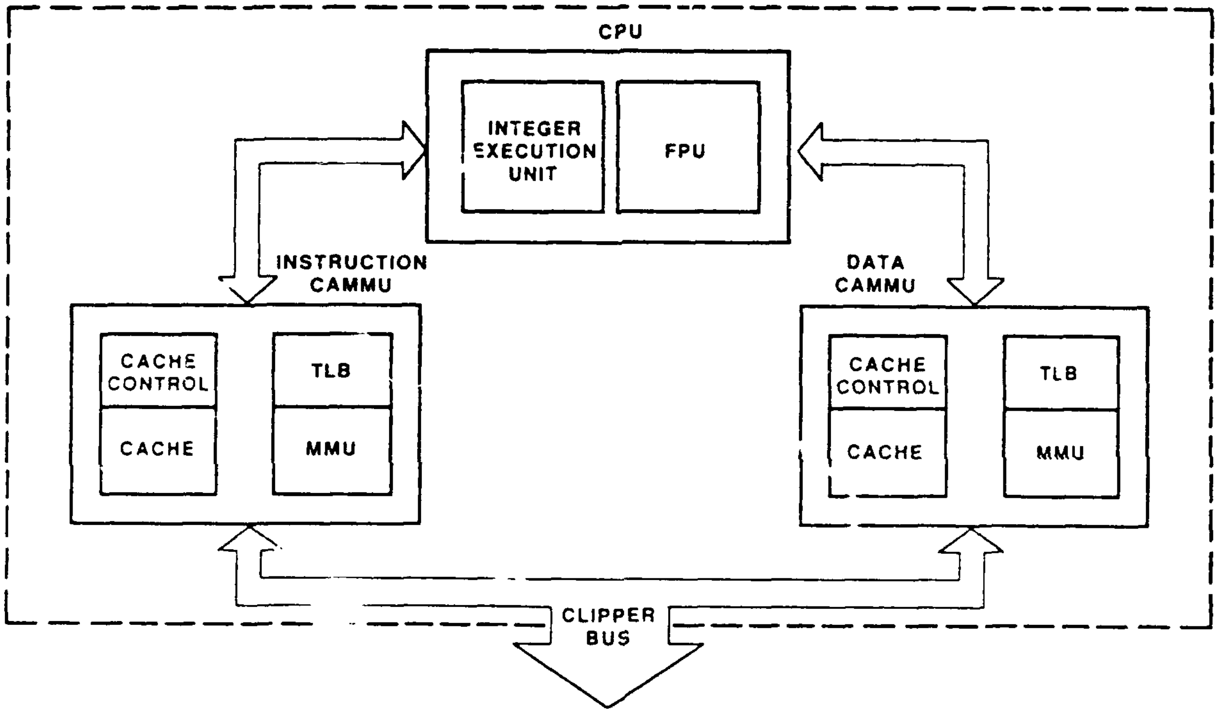
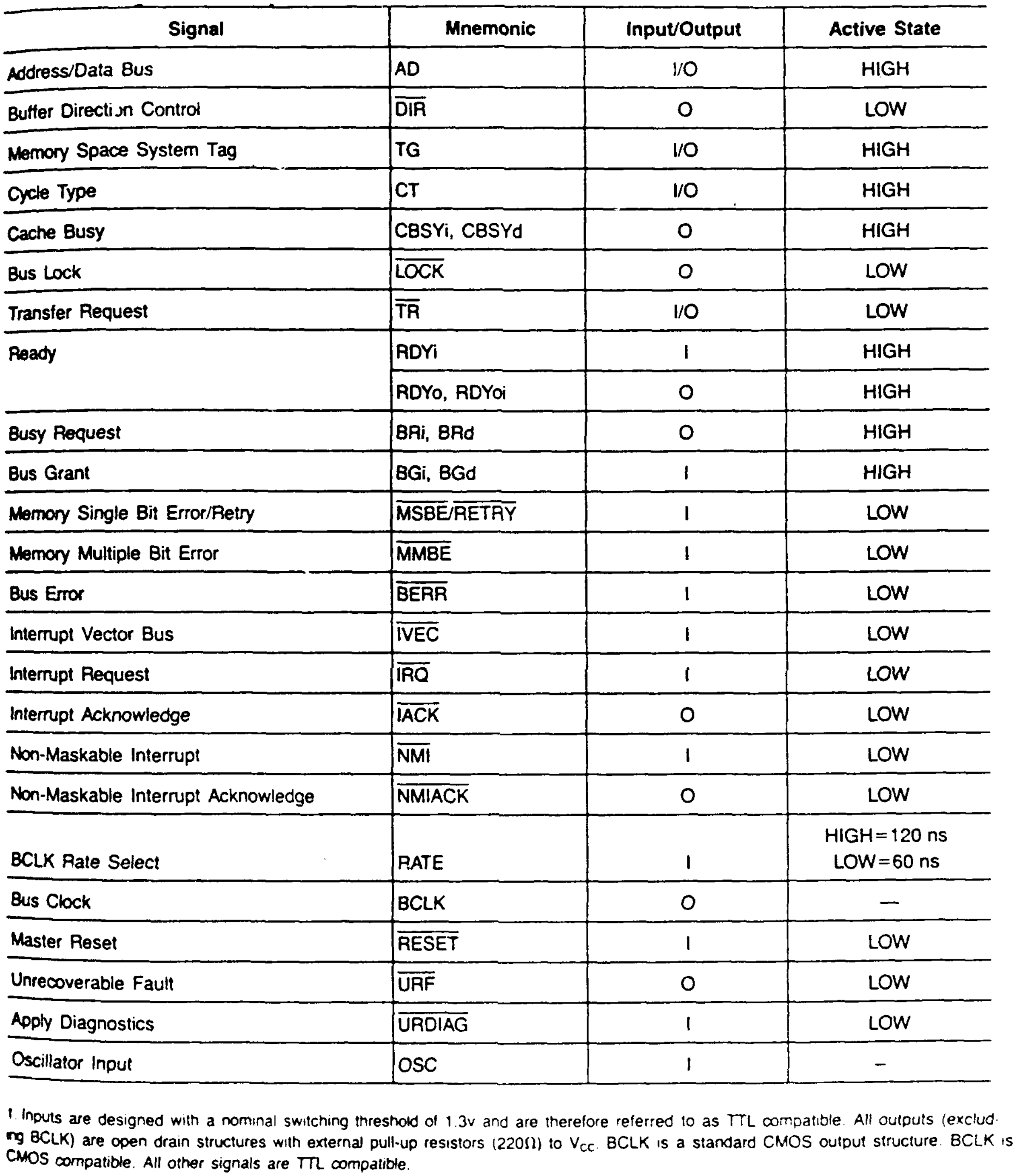


Figure 9-23. CLIPPER B!ɔck Diagram
(courtesy of Fairchild. CLIPPER^{TM} 32-bit Microprocessor: User's Manual, ©1987. Reprinted by permission of Prentice Hall, Fnglewood Cliffs, New Jersey.)



Signal	Mnemonic	Input/Output	Active State
Address/Data Bus	AD	I/O	HIGH
Buffer Direction Control	$\overline{DIR}$	O	LOW
Memory Space System Tag	TG	I/O	HIGH
Cycle Type	CT	I/O	HIGH
Cache Busy	CBSYi, CBSYd	O	HIGH
Bus Lock	$\overline{LOCK}$	O	LOW
Transfer Request	$\overline{TR}$	I/O	LOW
Ready	RDYi	I	HIGH
	RDYo, RDYoi	O	HIGH
Busy Request	BRi, BRd	O	HIGH
Bus Grant	BGi, BGd	I	HIGH
Memory Single Bit Error/Retry	$\overline{MSBE/RETRY}$	I	LOW
Memory Multiple Bit Error	$\overline{MMBE}$	I	LOW
Bus Error	$\overline{BERR}$	I	LOW
Interrupt Vector Bus	$\overline{IVEC}$	I	LOW
Interrupt Request	$\overline{IRQ}$	I	LOW
Interrupt Acknowledge	$\overline{IACK}$	O	LOW
Non-Maskable Interrupt	$\overline{NMI}$	I	LOW
Non-Maskable Interrupt Acknowledge	$\overline{NMIACK}$	O	LOW

BCLK Rate Select	RATE	I	HIGH=120 ns
			LOW=60 ns

Bus Clock	BCLK	O	—
Master Reset	$\overline{RESET}$	I	LOW
Unrecoverable Fault	$\overline{URF}$	O	LOW
Apply Diagnostics	$\overline{URDIAG}$	I	LOW
Oscillator Input	OSC	I	-

[1] Inputs are designed with a nominal switching threshold of 1.3v and are therefore referred to as TTL compatible. All outputs (excluding BCLK) are open drain structures with external pull-up resistors (220Ω) to V_{CC}. BCLK is a standard CMOS output structure. BCLK is CMOS compatible. All other signals are TTL compatible.

Figure 9-24. CLIPPER Signal Summary
(courtesy of Fairchild, CLIPPER^{TM} 32-bit Microprocessor: User's Manual, ©1987.
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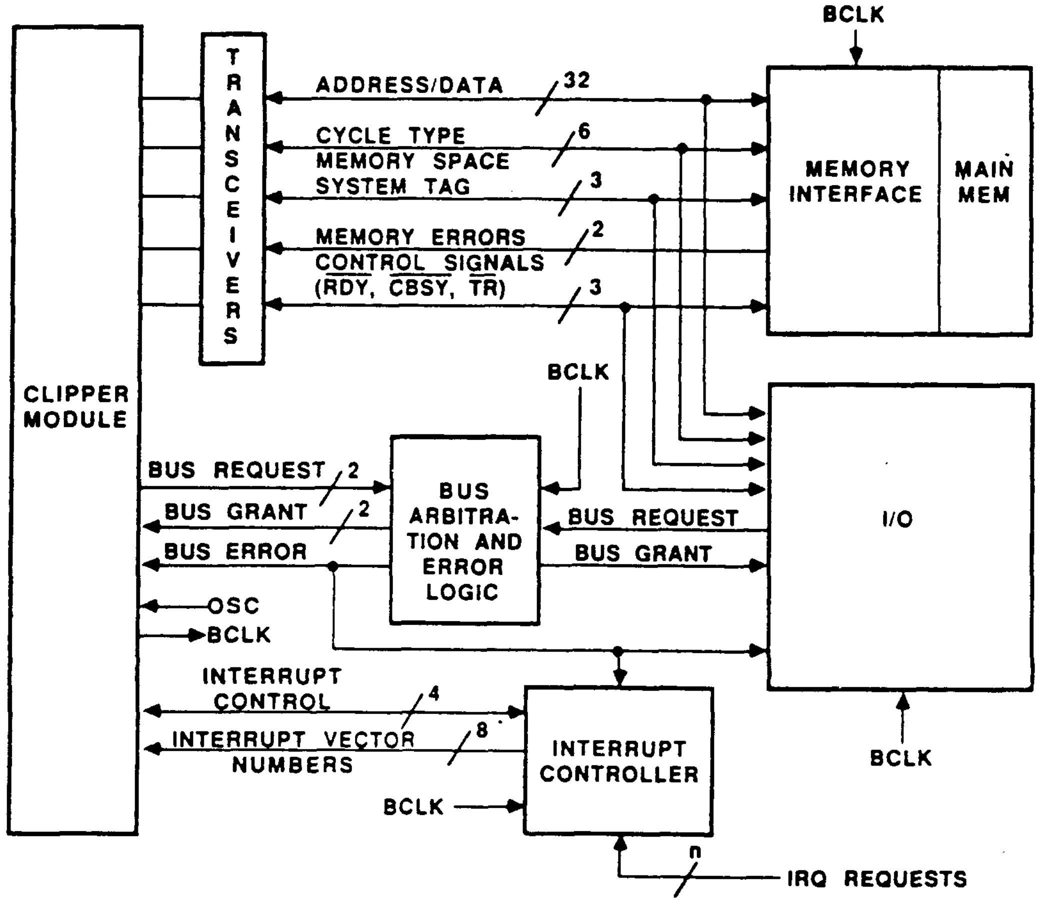

Figure 9-25. CLIPPER Block Diagram
(courtesy of Fairchild, CLIPPER^{TM} 32-bit Microprocessor: User's Manual, ©1987.
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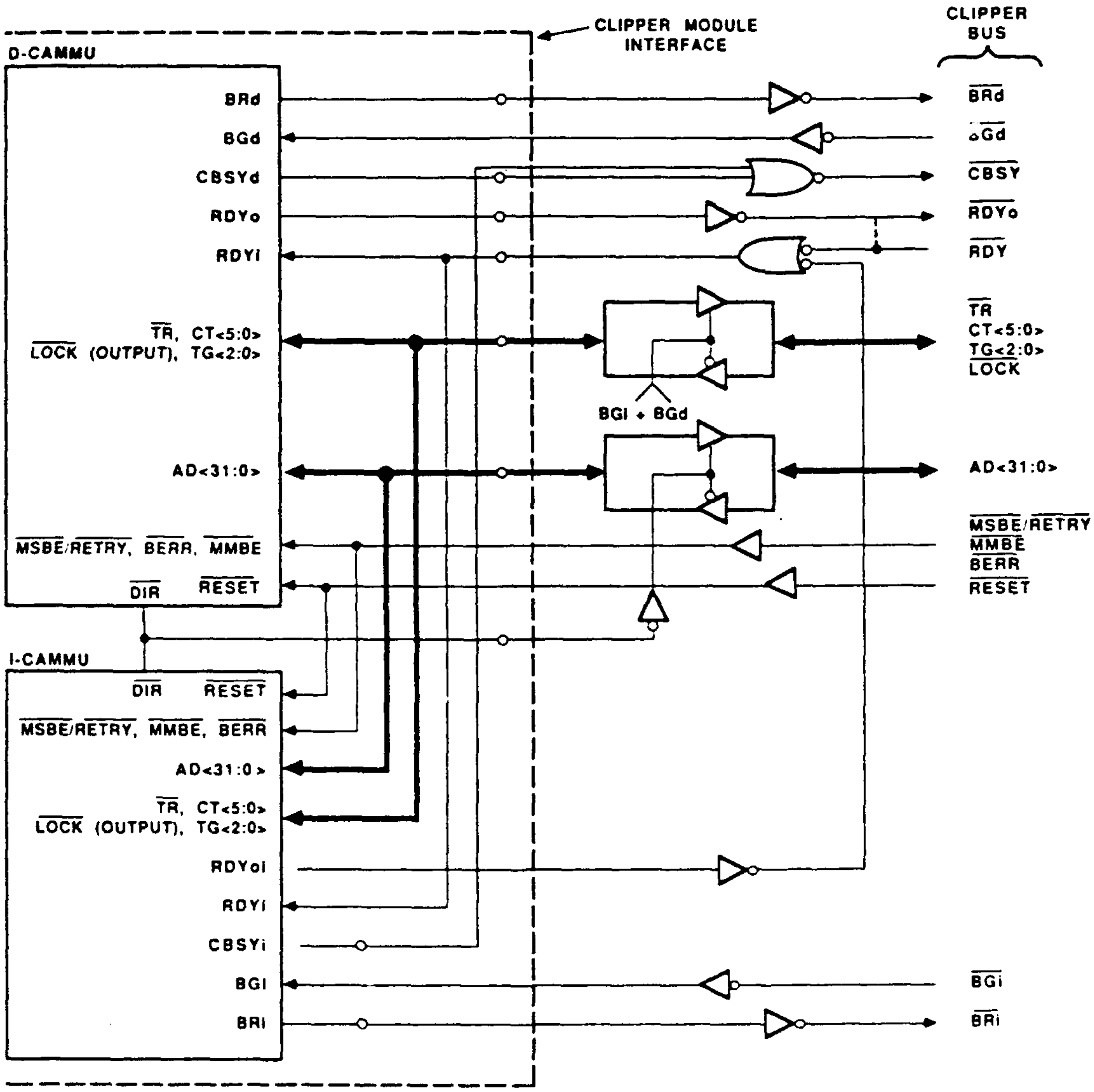


NOTES:

1 *Only signals between CAMMU and CLIPPER bus are shown This does not include interrupt signals* BCLK $\overline{\text{URF}}$ $\overline{\text{URDIAG}}$, or OSC
2 $\overline{\text{RDY}}$ and $\overline{\text{RDYo}}$ can connected together on the CLIPPER bus
3 —○— pullup resistor

Figure 9-26. CLIPPER Module Buffering
(courtesy of Fairchild, CLIPPER™ 32-bit Microprocessor: User's Manual, ©1987. Reprinted by permission of Prentice Hall, Englewood Cliffs, New Jersey.)

9.4.3.4.1 CLIPPER Diagnostics/Self Test. The following paragraphs on CLIPPER self-test and diagnostics were taken from the Fairchild, Inc., CLIPPER^{TM} data book, paragraph 7.2.8, 7.2.9, 7.2.9.1, and 7.3.2 (with the kind permission from Prentice Hall and Intergraph Corp). They show that the CLIPPER 32-bit microprocessor has an extensive self test capability.

9.4.3.4.1.1 Error Signals. The CLIPPER Bus offers effective means of error reporting and recovery with the Memory Single Bit Error/Retry /(MSBE/RETRY), Memory Multiple Bit Error (/MMBE), Bus Error (/BERR), and Unrecoverable Fault (/URF) signals.

Two types of system errors are most common: memory data errors, and bus errors.

1. Memory data errors are reported with the Memory Single Bit Error/Retry /(MSBE/RETRY) and the Memory Multiple Bit Error (/MMBE) signals. These signals are asserted by error detection and correction logic within the memory interface to indicate that a single bit error has been detected and corrected /(MSBE/RETRY), and that an uncorrectable multiple bit error has occurred (/MMBE). The signals, tied directly to the CAMMUs for fast response, force traps to error-handling routines. Note that the signals are asserted during the same cycle that RDYi is active.

   In cases of memory errors, the CAMMU Fault Register does not capture the addresses causing the errors. It is therefore necessary to design an address snapshot register into the system to capture addresses for use by the trap routines servicing the errors, if the addresses are required.

   The /(MSBE/RETRY) signal is also used to abort and retry CLIPPER Bus operations. If the signal is asserted during access of I/O space (TG=4) while RDYi is inactive, the current bus operation is aborted and retried with no trap assertion. This feature is intended to resolve deadlock in dual bus systems.

   The Memory Single Bit Error/Retry signal, therefore, operates as follows:

   - If the signal is asserted during any time other than access of I/O space and during the same clock cycle that RDYi is active, the signal reports a corrected memory single bit error. This causes the CAMMU to generate a trap to the CPU.

   - If the signal is asserted during access of I/O space (TG=4) while RDYi is inactive, the current bus operation is aborted and retried by the master CAMMU with no trap assertion to the CPU.

2. Bus errors are errors associated with bus operations. A common bus error is bus time out, which results when a bus slave fails to respond to a bus master within a define time. When such errors occur, the Bus Error (/BERR) signal should be asserted, which forces an abort of the current bus operation causing the error.

Bus Error is tied directly to each CAMMU. If a bus error occurs while a CAMMU is bus master, the CAMMU aborts the bus operation and releases the bus, but does not report the error condition to the CPU. Error should therefore be interfaced to an interrupt controller to force an interrupt to a bus error service routine when bus errors occur.

Some errors allow no clean means of recovery for continuation of program execution. These errors (unrecoverable faults) include the occurrence of a trap during execution of INTRAP or "reti", and the detection of a fault during self- test. A trap during execution of INTRAP or "reti" can be avoided by making sure that the Exception Vector Table is set up prior to the occurrence of a trap condition, and that the supervisor stack pointer always points to a valid page. No other conditions generate an unrecoverable fault.

Were the CPU to ignore these error conditions and continue execution, effects on the system could be catastrophic. A faulty or "lost" CPU could execute random writes to memory and I/O, for instance, corrupting data in both main memory and secondary storage.

The CLIPPER CPU offers protection from catastrophic failure by stopping program execution immediately upon detection of an unrecoverable fault condition, before the system is corrupted. It then asserts the Unrecoverable Fault signal (/URF) as a hardware indication that the CPU is halted due to an unrecoverable error, and that human intervention is required to correct the problem.

9.4.3.4.1.2 Reset and Diagnostics Control. The /RESET signal is asserted to force the CLIPPER Module to a known initialized state. It is normally asserted when power is initially applied to the CLIPPER Module, remains asserted for sufficient time to ensure full initialization, then is released to force instruction execution from Boot space.

Assertion of reset therefore places the CLIPPER Module in unmapped supervisor mode with all traps and conditional interrupts disabled. Also, all CLIPPER Bus active LOW signals are pulled HIGH (via pull-up resistors), and all active HIGH signals are forced LOW. BCLK continues clocking normally.

The state of Apply Diagnostics (/URDIAG) during the two BCLK cycles following release or reset determines whether the CLIPPER Module CPU executes internal diagnostics before executing from boot code.

This is a powerful feature of the module which allows self test of major functions of the CPU without test equipment, and without chip removal. Failure during diagnostics is reported by assertion of the Unrecoverable Fault (URF) CLIPPER Bus signal.

9.4.3.4.1.3 Self Test. The CLIPPER Module self test checks most major functions of the CPU, but not all. It is intended to be a first-level check of the CPU, which is in fact used to initially test individual CPU die during fabrication. The test executes approximately 700 instructions in about 4500 MCLK periods, using operands which test the CPU under worst-case conditions where possible. Worst-case carries, overflows, and sign extensions are tested, for example.

The following CPU operations and functions are tested:

1. Pipeline resource management.
2. Integer and Floating-Point execution units.
3. General purpose register files.
4. Integer bypass mechanism.
5. Transition between supervisor and user modes.
6. Temporary (hidden) registers.
7. Macro branches.
8. All addressing mode computations.
9. Arithmetic shift, logical shift, and rotate instructions.
10. Integer multiply and divide.
11. Single- and double-precision floating-point instructions.
12. Floating-point status bits.

CPU operations which require external response to instruction execution are not exhaustively tested. These include exception conditions, branches, loads, stores, pushes and pops, and I-CAMMU and D-CAMMU interfaces. For more detailed information, refer to the latest Intergraph Clipper data book.

9.4.3.4.2 Recommended Testability Access.

1. Control Lines
   - C300 CPU: /RDY, /CBSY, /TR, MEM ERR, /BRd, BRi, BCLK, /URF, /URDIAG, OSC
   - CAMMU: BGD, RDYi, /TR, /MSBE, /RETRY, /BERR, /MMBE, REST, BGi
2. Visibility Lines
   - C300 CPU: /BGi, /RESET, /(MSSE/RETRY), /MMBE, /BERR, /RDY, BGd
   - CAMMU: BRd, CBSYd, RDY, RDYoi, /LOCK, /DIR, CBSYi, bRi

9.5 Reduced Instruction Set Computer (RISC) Microprocessor.

The 32-bit CISC microprocessor market recently split into a subgroup called RISC (Reduced Instruction Set Computer).

What is a RISC microprocessor? The best way to describe a RISC microprocessor is to take a general CISC microprocessor and removing several of its internal parts including; the microcoded control store, the instruction decoder, the clock phase generator, the state machine logic, the CISC microprocessor control circuitry, the bus control, and the interrupt logic. The result is a branch that executes one instruction per cycle (the RISC microprocessor goal) and reduces the size and number of transistors needed making the overall chip smaller through a simplified design. An example: It took Intel more than 4 years to develop the 80386 CISC mircroprocessor, Motorola on the other hand developed its 88,100 and 88,200 RISC microprocessor chip set in approximately 20 months!

It should be noted here that RISC microprocessors have recently broken down into another subclass called SUPER SCALER microprocessor. These are processors that can execute more than one instruction per microprocessor clock cycle.

So far, RISC makers are avoiding the PC market because the existing applications software is linked so closely to the established Intel and Motorola CISC machines. However, a significant portion of the 32-bit workstations and scientific computer markets have committed themselves to RISC.

9.5.1 RISC Design/Testability Problems.

RISC based designs are not without their problems. The fastest RISC chip is only as efficient as the system it is built into. The ECL SPARC chip by BIT Corporation runs at 80 MHz. At these speeds it becomes absolutely critical to have a good interface to outside cache and have a clean and precise cycle relationship. This becomes extremely difficult when the memory speed is exactly the same as the processor speed.

At these speeds all board interconnects became transmission lines. Also most other chip peripherals do not fit well with RISC processors.

Test points must be designed into these boards at the very beginning since board lead impedances and parasitic capacitances can add multiple nanosecond delays that these designs cannot afford.

Also system memories must be carefully matched to the processor speed.

9.5.2 The Motorola 88000 Family.

Motorola's first version of the RISC family microprocessor is the M88000 family using Motorola HCMOS technology. The 88000 family has the features needed for CPUs in work stations and computers including separate data and instruction buses giving a maximum throughput.

The minimum configuration for this microprocessor set is one 32-bit CPU (88100) chip and two cache/memory management units (CMMU) chips (88200s). The CMMUs add high-speed memory caching, two-level demand-paged memory management, and support for shared memory multi-processing. See figure 9-27 and figure 9-28 for system block diagrams. This 3-chip set is remarkably similar to the Intergraph CLIPPER microprocessor.

Figures 9-29 and 9-30, give the block diagram of the individual chips. For more detailed information, see Motorola's M88100 and M88200 data books.

9.5.2.1 Testability Control/Visibility Points.

- Control lines include:
  - For the 88100: DRO, DRI, CRO, CR1, INT, /RST, PLLEN, CLK, PCE
  - For the 88200: S/(not)U, R/(not)W, /DLOCK, DBE0-3, BG, /BB, /AB, MCE, /RST, /PCS, PCE, SRAMMODE, /(SS3-SS0), CLK, PLLEN, Vcc, GRND
- Visibility or test points include:
  - For the 88100: CFETCH, CS/(not)U, ERR, DS/(not)U, DR/(not)W, /DLOCK, DBE0:3
  - For the 88200: R0, R1, ST3:0, TM0, TR0, TR1, BR, BA, ERR

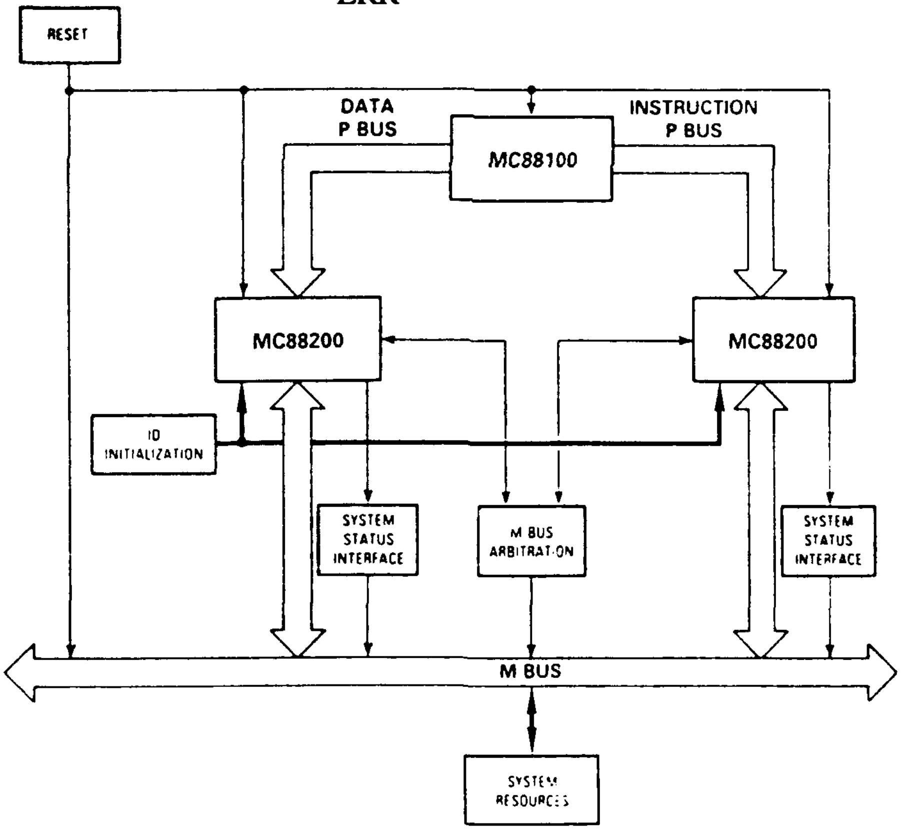


Figure 9-27. 88000 Family Basic System Configuration
(courtesy of Motorola MC88100: User's Manual, ©1990, pp. 8-2. Reprinted by permission of Prentice Hall, Englewood Cliffs, New Jersey.)

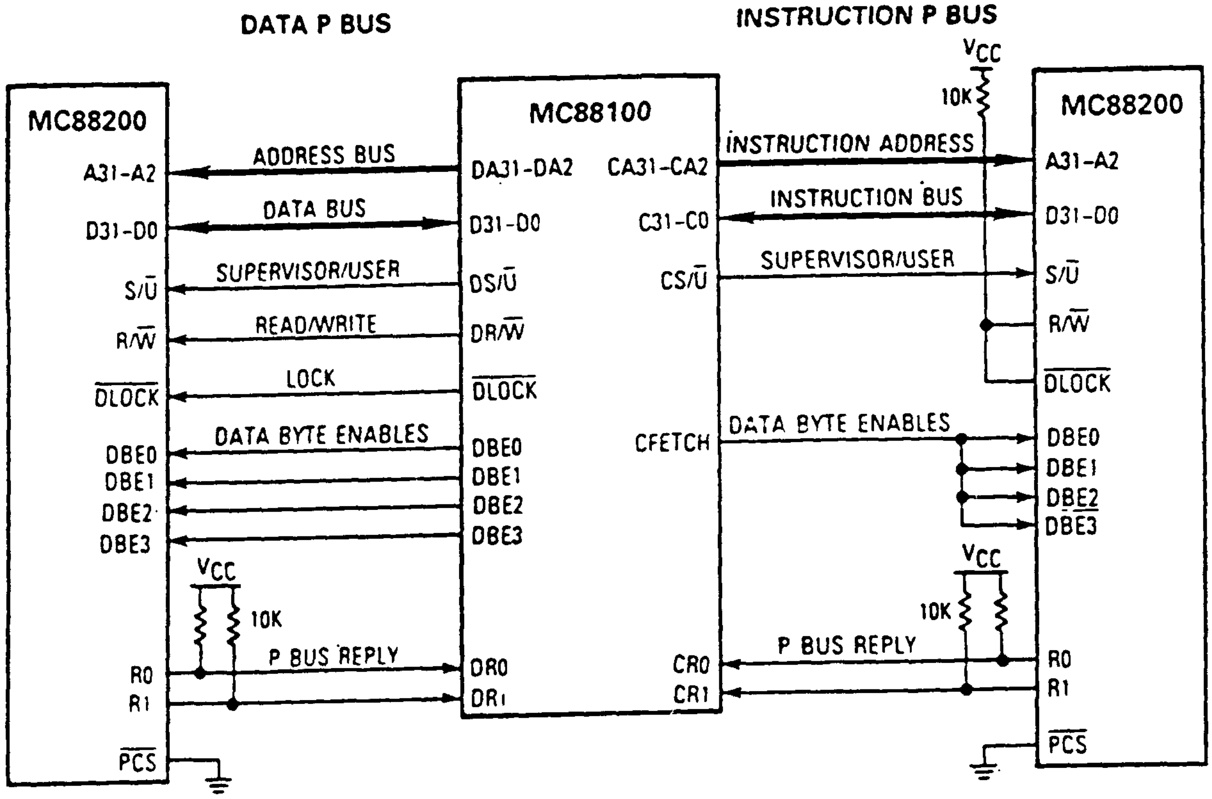
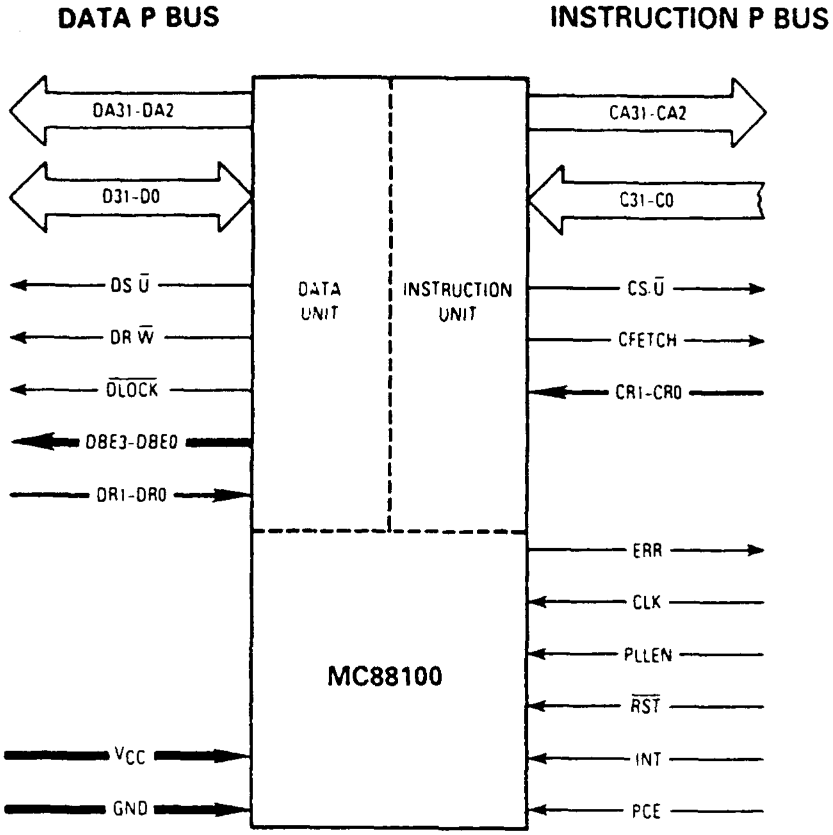


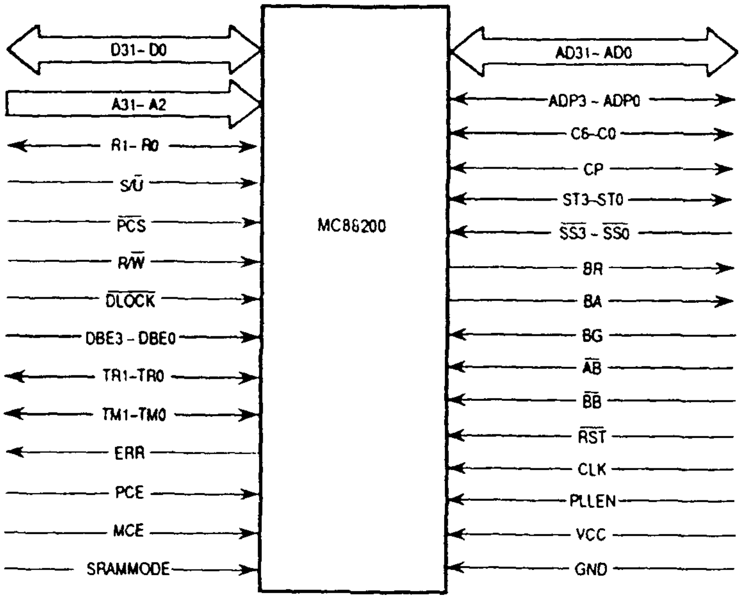
Figure 9-28. Basic Connections Between One 88100 and Two 8200s (courtesy of Motorola MC88100: User's Manual, ©1990, pp. 8-3. Reprinted by permission of Prentice Hall, Englewood Cliffs, New Jersey.)



Function	Mnemonic	Type	Active	Count	Reset
Data Address	DA31-DA2	Output	—	30	High Impedance*
Data	D31-D0	I O	—	32	High Impedance*
Data Supervisor User Select	DS Ū	Output	—	1	High Impedance*
Data Read Write	DR W̄	Output	—	1	High Impedance*
Data Bus Lock	$\overline{DLOCK}$	Output	Low	1	High Impedance*
Data Byte Enable	DBE3-DBE0	Output	High	4	High Impedance*
Data Reply	DR1-DR0	Input	—	2	Input
Code Address	CA31-CA2	Output	—	30	High Impedance*
Code	C31-C0	Input	—	32	High Impedance*
Code Supervisor User Select	CS Ū	Output	—	1	Input
Code Fetch	CFETCH	Output	High	1	High Impedance*
Code Reply	CR1-CR0	Input	—	2	Input
Error	ERR	Output	High	1	Low
Reset	$\overline{RST}$	Input	Low	1	Input
Interrupt	!NT	Input	High	1	Input
P Bus Checker Enable	PCE	Input	High	1	Input
Clock	CLK	Input	High	1	Input
Phase Lock Enable	PLLEN	Input	High	1	Input
Power	V_{CC}	—	—	18	—
Ground	GND	—	—	18	—

*These signals remain in the high-impedance state for one clock cycle after the $\overline{RST}$ signal is recognized as negated (high)

Figure 9-29. Functional Block Diagram of MC8810
(courtesy of Motorola MC88100: User's Manual, ©1990, pp. 4-2. Reprinted by permission of Prentice Hall, Englewood Cliffs, New Jersey.)



Function	Mnemonic	Type	Active	Count	Reset State
P Bus					
Address	A31 - A2	Input	High	30	Ignored
Supervisor User	S $\overline{\text{U}}$	Input	High	1	Ignored
Chip Select	$\overline{\text{PCS}}$	Input	Low	1	Ignored
Data Byte Enable	DBE3-DBE0	Input	High	4	Ignored
Data	D31 -D0	I O	High	32	High Impedance
Read Write	R $\overline{\text{W}}$	Input	High	1	Ignored
Lock	$\overline{\text{DLOCK}}$	Input	Low	1	Ignored
Reply	R1-R0	I O	High	2	High Impedance
M Bus					
Bus Request	BR	Output	High	1	Negated
Bus Grant	BG	Input	High	1	Ignored
Bus Acknowledge	BA	Output	High	1	Negated
Arbitration Busy	$\overline{\text{AB}}$	Input	Low	1	Ignored
Bus Busy	$\overline{\text{BB}}$	Input	Low	1	Ignored
Address Data	AD31 - AD0	I O	High	32	High Impedance
Address Data Parity	ADP3 - ADP0	I O	High	4	High Impedance
Control	C6-C0	I O	High	7	High Impedance
Control Parity	CP	I O	High	1	High Impedance
Local Status	ST3-ST0	I O	High	4	Active Input
System Status	$\overline{\text{SS3}}$-$\overline{\text{SS0}}$	Input	Low	4	Ignored
Reset	$\overline{\text{RST}}$	Input	Low	1	Asserted
Clock	CLK	Input	High	1	Active
Phase Lock Enable	PLLEN	Input	Low	1	Active
Tag Monitor	TM1-TM0	I O	High	2	Active Input
Trace	TR1-TR0	I O	High	2	Active Input
Cache Static RAM Mode	SRAMMODE	Input	High	1	Active Input
P Bus Checker Enable	PCE	Input	High	1	Active Input
M Bus Checker Enable	MCE	Input	High	1	Active Input
Error	ERR	Output	High	1	Low
Power	VCC			18	
Ground	GND			18	

Figure 9-30. Functional Block Diagram of MC88200 Signals (courtesy of Motorola MC88200: User's Manual, ©1989, pp. 4-2. Reprinted by permission of Prentice Hall, Englewood Cliffs, New Jersey.)

9.5.3 Scaleable Processor Architecture (SPARC) 32-Bit (RISC) Microprocessor. The SPARC architecture is the only multiple-sourced RISC processor architecture in the world that is openly licensable. There are presently SPARC microprocessor gate arrays, custom CMOS, ECL, and GaAs versions available. Over two hundred application software packages are now available on SPARC. This is the only RISC chip that has software allowing it to emulate both MS-DOS and VAX/VMS running all of the applications software for these environments. Consequently, the SPARC CPU has more available application source code running at this time then all other RISC microprocessors combined. 80 companies world wide have all committed to the SPARC RISC microprocessor including CYPRESS Semiconductor, AT&T, UNISYS, SYN, XEROX, and FUJITSU. The CYPRESS Semiconductor CMOS 7C601 can run at 33 MHz, 24 MIPS. (See figures 9-31 and 9-32).

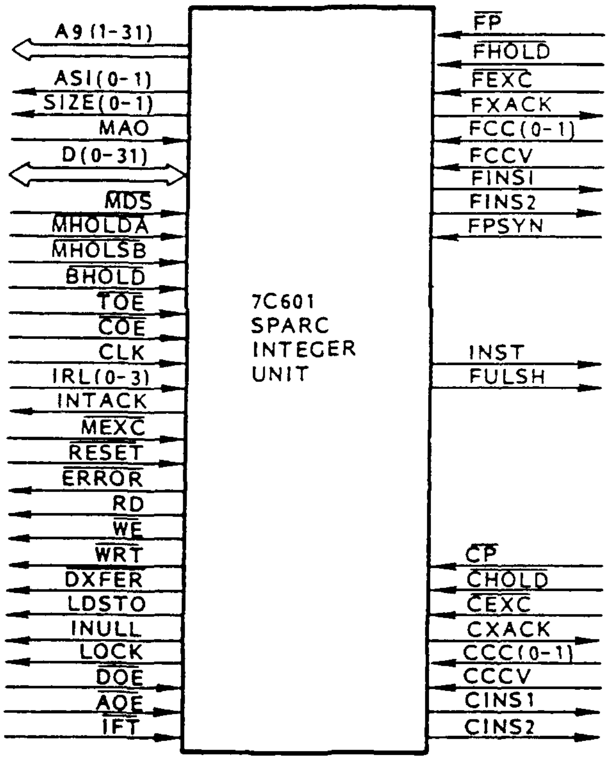


Figure 9-31. 7C601 SPARC (CPU) Integer Unit
(courtesy of Cypress Semiconductor)

One problem with the SPARC licensing agreement is that different SPARC manufacturers use different pin configurations.

The fastest SPARC design to date is Bipolar Integrated Technology's ECL SPARC version running at 80 MHz.

The SPARC International consortium of hardware and software vendors is dedicaied to creating and maintaining open standards and multiuser compatibility of SPARC-based machines and applications.

9.5.3.1 7C600 SPARC 32-Bit RISC CPU Family (CYPRES Semiconductor). The SPARC CPU chip set is composed of a 7C601 Integer Unit (IU) or CPU and a 7C608 Floating Point Controller (FPC) which can interface to any of a number of standard floating units that perform floating point calculations.

Although not a formal part of the architecture, 7C600-based computers can have a memory management unit (MMU), a large virtual-address cache for instructions and data, and are organized around a 32-bit data and instruction bus.

The integer and floating-point units operate concurrently. The FPU performs floating-point calculations with a set number of floating-point arithmetic units. The 7C600 architecture also specifies an interface for the connection of an additional coprocessor.

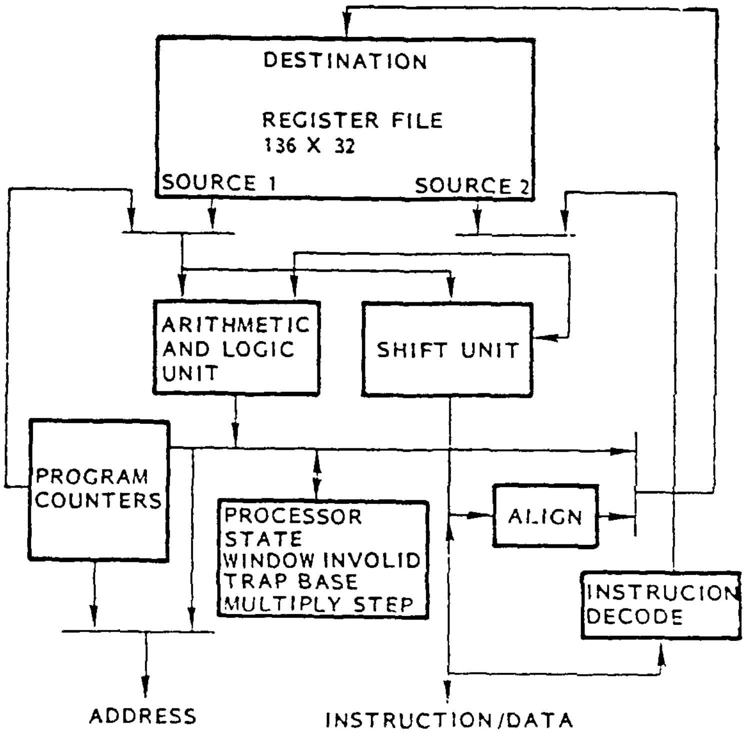


Figure 9-32. CY7C601 SPARC (CPU) Integer Unit Block Diagram (courtesy of Cypress Semiconductor)

9.5.3.2 7C601 Testability Control/Visibility Points.

1. Control lines include:

   - For 7C601 (IU) MAO, /MDS, /MHOLDA, /MHOLDB, /BHOLD, /TOE, /COE, CLK, IRL(0-3), /MEXC, /RESET, /DOE, /AOE, /IFT, /FP, /FHOLD, /FEXC, FCC(0-1), FCCV, FPSYN, CP, CHOLD, /CEXC, CCC(0-1), CCCV

2. Visibility lines or Test Points include:

   - For 7C601(IU) ASI(0-1), SIZE(0-1), INTACK, /ERROR, RD, /WE, WRT, DXFER, LDSTO, INULL, LOCK, FXACK, FINS(1-2), INST, FLUSH, CXACK, CINS(1-2)

9.5.3.3 CY7C608 (FBC) Testability Control/Visibility Points.

- Control lines include:

  - For CY7C608 (FPC) FXACK, FINS(1-2), INST, FLUSH, CCCV, /CHOLD, /TOE, /MHOLD, /A-C, /MDS, /DOE, /FPRES, CHAIN, /RESET, CLK,

  TEST 0-1, RESULT BUS, STATUS 0-11.

- VISIBILITY lines or Test Points include:

  - For CY7C608 (FPC) EST 0-1, INSTR BUS, /RESET /ENA, OPERAND 0-1, RND-MD 0-1, SELECT 0-2, CCLK, STALL, /FP, FCCV, FCC 0-1, /FHOLD, /FEXC.

9.5.4 MIPs Microprocessor (RISC) 32-Bits). The MIPS (microprocessor without Interlocking Pipeline Stages) from the MIPS company was the first RISC microprocessor to be shipped in 1985. Today dozens of system companies market products based on the MIPS design, which is now owned by the Intergraph Device Technology Corporation.

The R6000 is the most advanced MIPS chip available. It is the ECL version of the R3000. Recently the R3000 (see figures 9-33 and 9-34) was selected a standard microprocessor in military avionics programs by JIAWG (Joint Internal Avionics Working Group). It is being used by the Advanced Tactical Fighter Program. It achieves 28 MIPS.

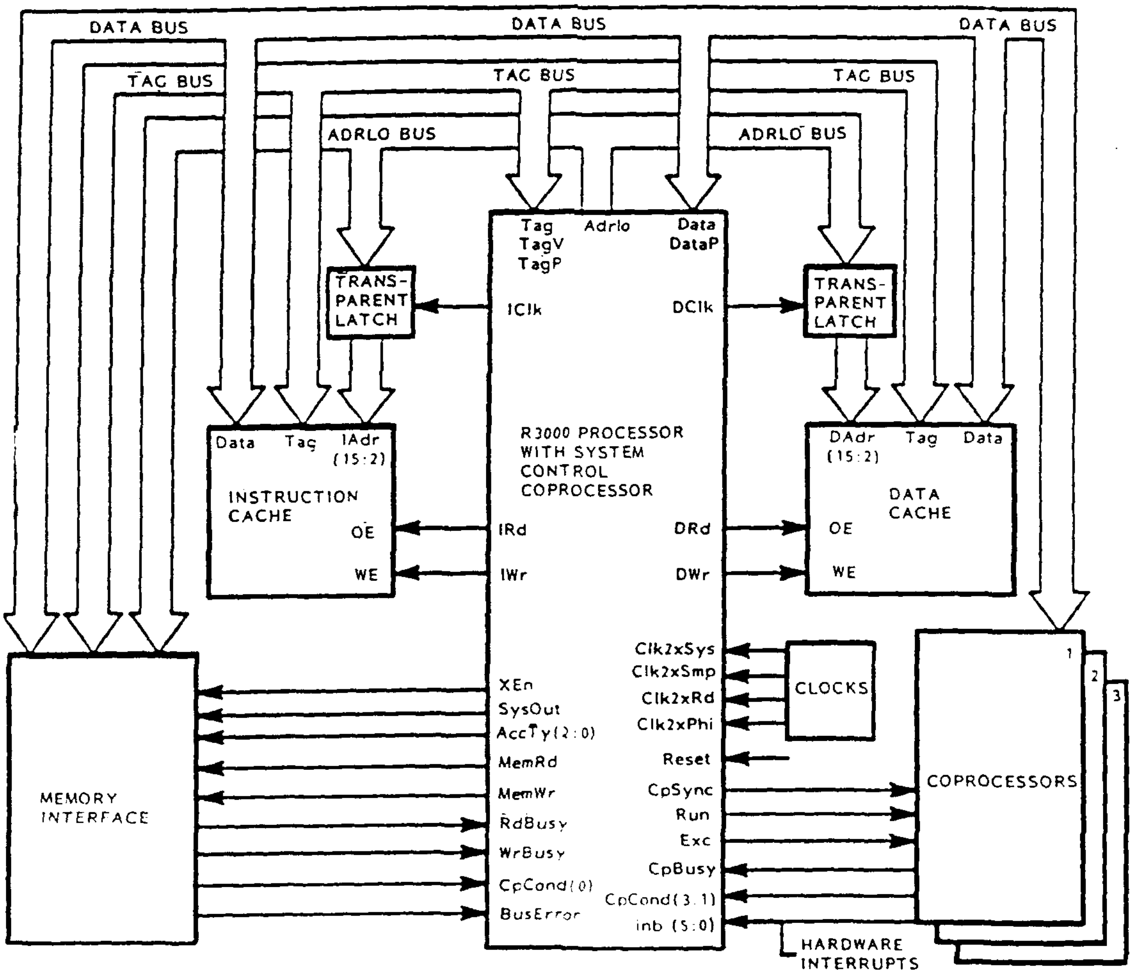


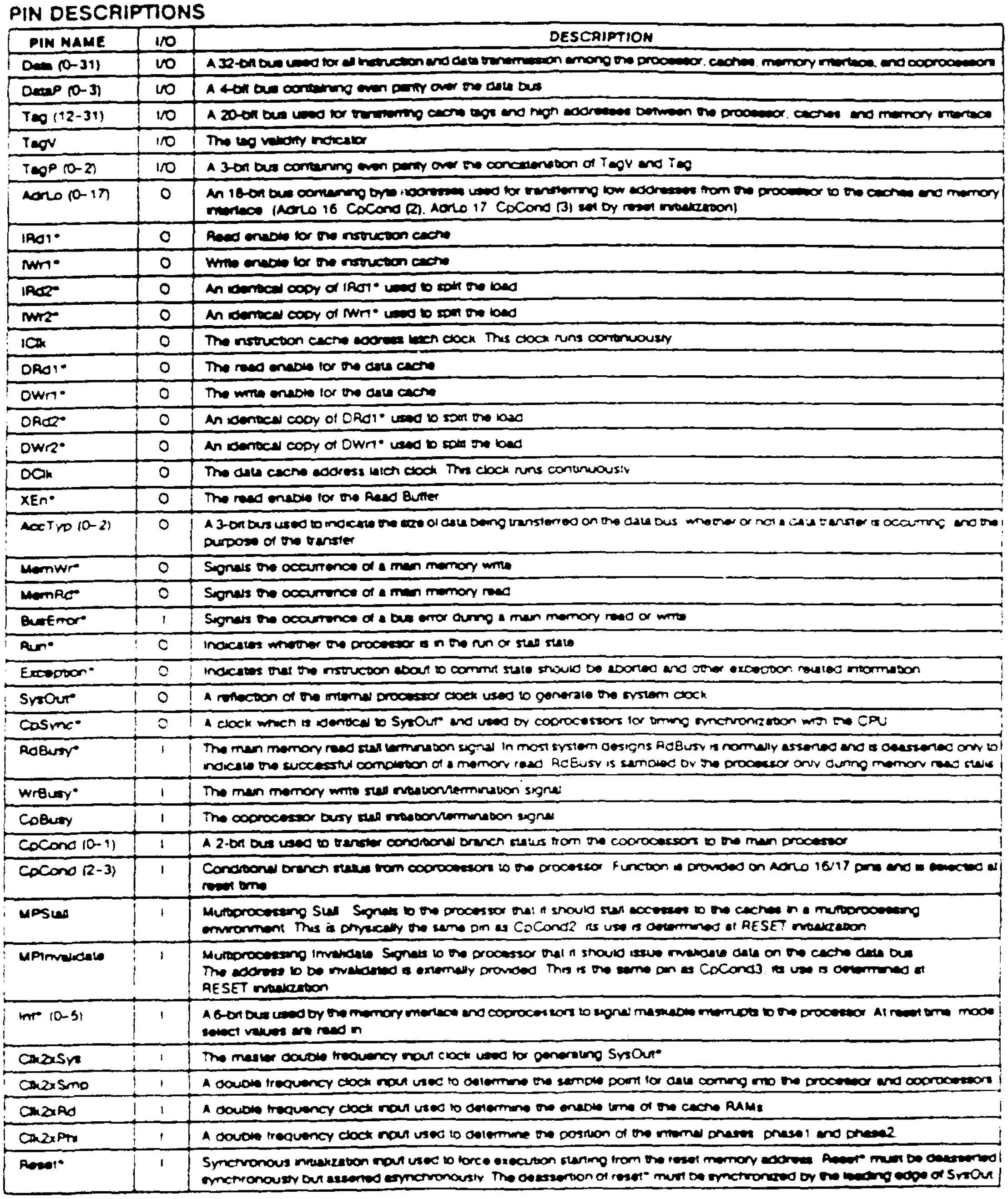
Figure 9-33. R3000 Processor Block Diagram
(courtesy of Integrated Device Technology Corp.)

The R6000 is capable of a 50 MIPS performance. This version is software compatible with its earlier CMOS R2000, and R3000 microprocessors. It processes one instruction per cycle which at 50 MIPS means the instruction is only 20 ns long.

This means cache memory needs to be high speed RAM of 15 ns or better access time.

Both the R2000/R3000 (R6000) are multi-sourced processors. This processor was originally developed at Stanford for DARPA to deliver 28 MIPS (million instructions per second).

The R3000 is instruction set compatible with the MIPS R2000 processor. The principle differences between the R3000 and the R2000 are in the memory interface.For detailed R3000/R2000 differences see Integrated Device Technology High Performance CMOS DATA BOOK, Supplement 1989.



PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
Data (0-31)	I/O	A 32-bit bus used for all instruction and data transmission among the processor, caches, memory interface, and coprocessors
DataP (0-3)	I/O	A 4-bit bus containing even parity over the data bus
Tag (12-31)	I/O	A 20-bit bus used for transferring cache tags and high addresses between the processor, caches and memory interface
TagV	I/O	The tag validity indicator
TagP (0-2)	I/O	A 3-bit bus containing even parity over the concatenation of TagV and Tag
AdrLo (0-17)	O	An 18-bit bus containing byte addresses used for transferring low addresses from the processor to the caches and memory interface (AdrLo 16 CpCond (2), AdrLo 17 CpCond (3) set by reset initialization)
IRd1*	O	Read enable for the instruction cache
IWr1*	O	Write enable for the instruction cache
IRd2*	O	An identical copy of IRd1* used to split the load
IWr2*	O	An identical copy of IWr1* used to split the load
IClk	O	The instruction cache address latch clock This clock runs continuously
DRd1*	O	The read enable for the data cache
DWr1*	O	The write enable for the data cache
DRd2*	O	An identical copy of DRd1* used to split the load
DWr2*	O	An identical copy of DWr1* used to split the load
DClk	O	The data cache address latch clock This clock runs continuously
XEn*	O	The read enable for the Read Buffer
AccTyp (0-2)	O	A 3-bit bus used to indicate the size of data being transferred on the data bus whether or not a data transfer is occurring and the purpose of the transfer
MemWr*	O	Signals the occurrence of a main memory write
MemRd*	O	Signals the occurrence of a main memory read
BusError*	I	Signals the occurrence of a bus error during a main memory read or write
Run*	O	Indicates whether the processor is in the run or stall state
Exception*	O	Indicates that the instruction about to commit state should be aborted and other exception related information
SysOut*	O	A reflection of the internal processor clock used to generate the system clock
CpSync*	O	A clock which is identical to SysOut* and used by coprocessors for timing synchronization with the CPU
RdBusy*	I	The main memory read stall termination signal In most system designs RdBusy is normally asserted and is deasserted only to indicate the successful completion of a memory read RdBusy is sampled by the processor only during memory read stalls
WrBusy*	I	The main memory write stall initiation/termination signal
CpBusy	I	The coprocessor busy stall initiation/termination signal
CpCond (0-1)	I	A 2-bit bus used to transfer conditional branch status from the coprocessors to the main processor
CpCond (2-3)	I	Conditional branch status from coprocessors to the processor Function is provided on AdrLo 16/17 pins and is selected at reset time
MPStall	I	Multiprocessing Stall Signals to the processor that it should stall accesses to the caches in a multiprocessing environment This is physically the same pin as CpCond2 its use is determined at RESET initialization
MPInvalidate	I	Multiprocessing Invalidate Signals to the processor that it should issue invalidate data on the cache data bus The address to be invalidated is externally provided This is the same pin as CpCond3 its use is determined at RESET initialization
Int* (0-5)	I	A 6-bit bus used by the memory interface and coprocessors to signal maskable interrupts to the processor At reset time mode select values are read in
Clk2xSys	I	The master double frequency input clock used for generating SysOut*
Clk2xSmp	I	A double frequency clock input used to determine the sample point for data coming into the processor and coprocessors
Clk2xRd	I	A double frequency clock input used to determine the enable time of the cache RAMs
Clk2xPhi	I	A double frequency clock input used to determine the position of the internal phases phase1 and phase2
Reset*	I	Synchronous initialization input used to force execution starting from the reset memory address Reset* must be deasserted synchronously but asserted asynchronously The deassertion of reset* must be synchronized by the leading edge of SysOut

Figure 9-34. Pin-Out Description of R3000 (R6000)
(courtesy of Integrated Device Technology Corp.)

9.5.4.1 Testability Control/Visibility Points.

- Control lines include:

  For R3000 (R6000): /RdBUSY, WrBUSY; CPCOND(0), BUS ERROR, INTR(5:0), CpCOND(3:1), CP BUSY, REST, CLK2XPH, /CLK2XRd, CLKZXSMP, CLK2XSYS,

- Visibility lines or Test Points include:

  For R3000 (R6000): ICLK, DCLK, DRd; DWR, CpSYNC; RUN; EXC; MEMWR, MEMRd, ACCTY(2:D), SYSOUT, XEN, IRd, IWR, DWR2, DRd2, DRd1, DWR1, IRd(1-2), IWR(1-2).

9.6 Transputers (INMOS CORP).

Transputer architectures are non-Von Newman microprocessors aimed at parallel processing (manufactured by INMOS Corporation a subsidiary of SGS Thompson Corp.). Each TRANSPUTER chip includes an integer processor, a certain amount of fast memory, a floating point unit (FPU) and multiple serial communication links providing point to point communication links between transputers.

Link communications run simultaneously with processor computation and require no processor overhead. Thus literally hundreds can be linked together linearly increasing their performance speed with no theoretical limit.

One chip = 25 MIPS, 2 chips = 50 MIPS, 10 chips tied in parallel deliver 250 MIPS.

Two types of transputers presently exist, the IMS T425 and the IMS T800. The T800 is 12 times faster then the Intel 80386 and gives 6 times the performance of the 68020/68881 combination.

A 30 MHz IMS T800 has a typical power dissipation of only 680 mW. The package only has 84 pins in a PGA that is 1.06 square. The IMS T800 comes in a 3.5 inch x 1 inch module called a TRAM which incorporates not only the T800 but also 1 MBYTE DRAM.

Ten of these TRAMS can be plugged into an IMS B008 motherboard for the IBM PC-XT or AT. (TRAMS have become an industry standard for plugging together parallel microprocessors).

Transputer development tools are available in a special software language called OCCAM developed especially for parallel processing.

C, FORTRAN, ADA, and PASCAL compilers including parallel versions are also available from different sources.

Tool sets are available for IBM, SUN, and VAX machines.

9.6.1 Transputer Testability. Testability of these chips seem difficult in that data/addresses are multiplexed, but the transputers can be bootstrapped with diagnostic software.

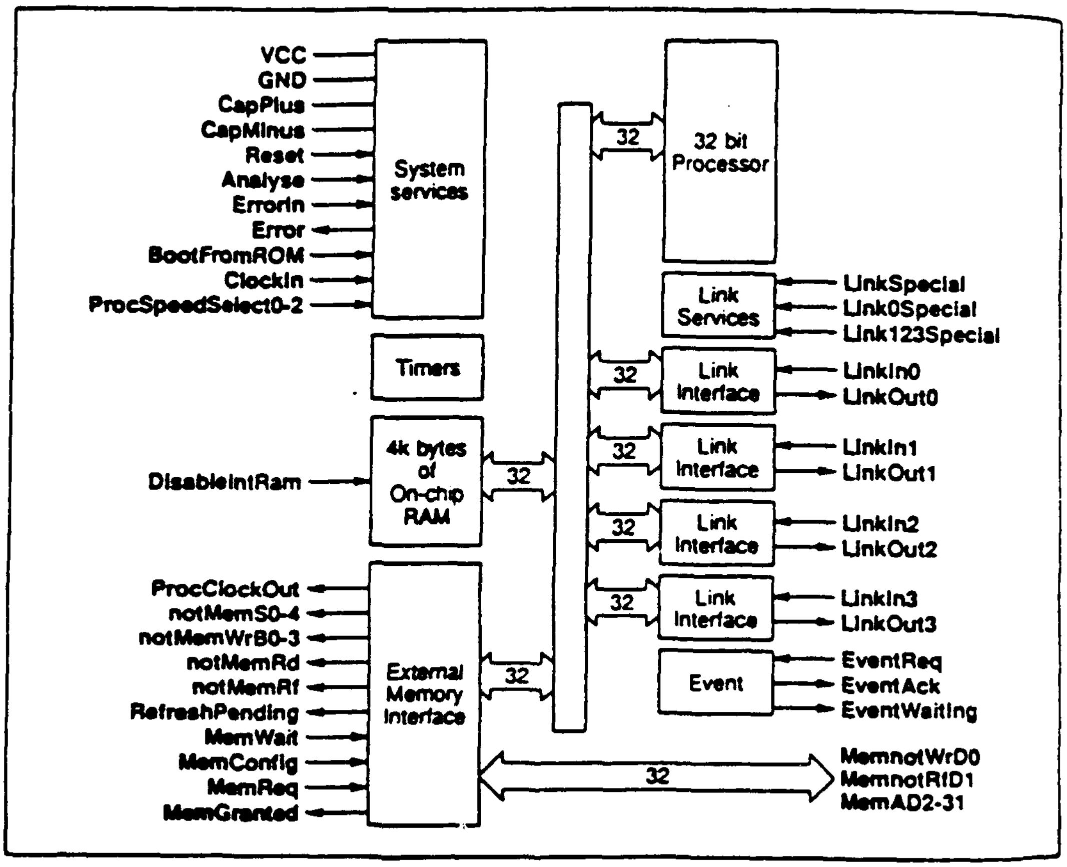


Figure 9-35. T425 Block Diagram
(by courtesy of SGS-Thompson Microelectronics.)

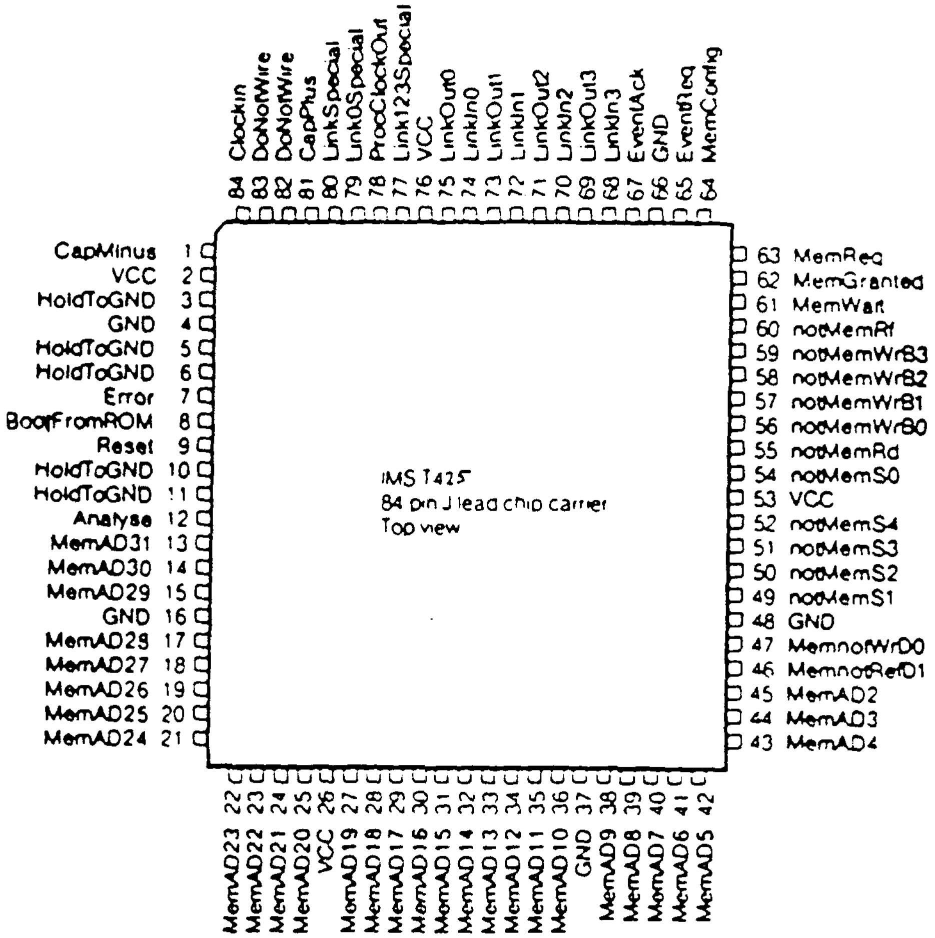


Figure 9-36. T425, 84 Pin J-Lead Chip Carrier Version
(by courtesy of SGS-Thompson Microelectronics.)

9.6.2 Testability Control/Visibility Points

- Control lines include:

  For T425: MESSAGE, MEM CONFIG, CLOCK IN, RESET, ANALYSE, BOOT FROM ROM, CAP PLUS, LINKIN 0-3

- Visibility lines on Test Points include:

  For T425 : MEM WAIT, MEM GRANT, MEM NOT RrfD1, MEM NOT WrDO, NOT MEMS(0-4), NOT MEM Rf, NOT MEM Rd, NOT MEMWRB(0-3), LINK OUT (0-3)

9.7 Bit Slice Microprocessor.

Bit Slice technology was originally used in embedded systems for optimum bit length designs. They were always difficult to use since one had to develop software for programming them using assembly language, making design and developing tests for them difficult. The 2901 has been the traditional work horse in this arena and is reviewed here. Recently the 29C00 (CMOS) and the 29G00 80 MHz GaAs version have been introduced. But their basic pin outs are the same. It is second sourced by many different companies even with an ECL version.

9.7.1 The 2901. The original 2901 is a bit slice microprocessor that is not dynamic in nature, as it can run asynchronously. 2901-based printed circuit boards do not normally require refresh circuitry (with its attendant testability problems), unless dynamic RAM is used elsewhere in a system design.

The pin-out for the 2901 dip package is shown in figure 9-37.

Each package features a 4-bit data input, 4 bit data output (which is tri-stateable), RAM address and shift logic inputs plus several status and control lines.

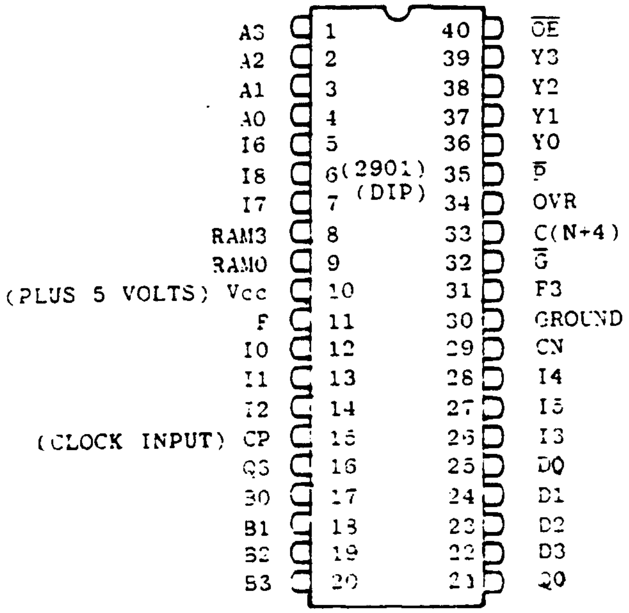


Figure 9-37. 2901 (DIP)

The key guideline to testability of a board using 2901 devices is individual control of the /OE (output enable) lines. With control, each device can first be individually exercised prior to the full functional test of the board.

Access should also be provided to the following common line:

D0-D3	Data input lines
Y0-Y3	Data output lines
A0-A3	Local RAM A address Lines
B0-B3	Local RAM B address lines
RAM-RAM3	RAM shift logic
Q0-Q3	Q register shift logic
CH	Carry in
CP	Clock pulse input
F	Zero status

The Y0-Y3 lines are tri-state lines and should have pull-up resistors attached to the common bus. This same guideline holds true for the F output, which is an open collector output.

The ability to control individual /OE lines should not be overemphasized from a testing standpoint. This control allows a partitioned testing approach reducing the need for 2901 microcode for a complete board test. This reduces the effort for software initialization of the A and B latches and Q registers.

9.7.2 The 2903. The 2903 (pin-out shown in figure 9-38) has the same input ports as the 2901 (/DA0-/DA3), with two bidirectional output data ports (DB0-DB3 and Y0-Y3).

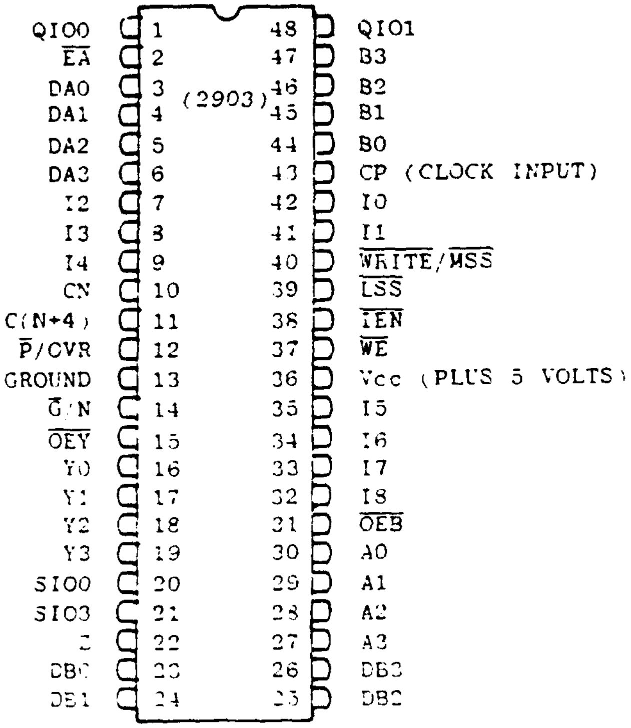


Figure 9-38. 2903 (DIP)

Testability guidelines for the 2903 include those mentioned for the 2901, and also include need for control and access points at:

/EA
/OEB
/EN
/WE
/OEY
/LSS

9.7.3 The 2902. The 2902 carry look ahead device creates parallel carry inputs for slices beyond the least significant slice. The pin-out is shown in 9-39.

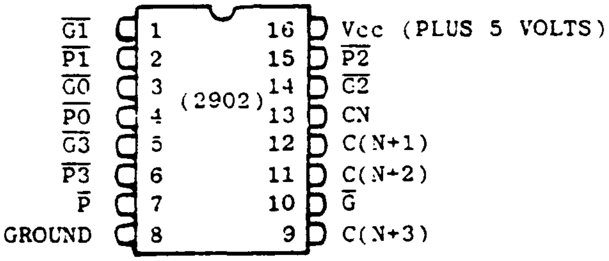


Figure 9-39. 2902 (DIP)

This device is tested as part of the 2901/2901 system design and cannot be isolated.

9.7.4 The 2910. The 2910 microprogram sequencer (pin-out not illustrated) requires control point access to the CCEN (condition code enable) and OE (output enable) lines. The CP (clock pulse) is synchronous with other 29XX devices.

9.7.5 The 2930 and 2932. The 2930 and 2932 program control units are architecturally similar to the 2901, with Q register functions modified to operate as a local data register, and the local RAM used as a stack internal to the devices.

9.7.6 Bit Slice Summary. The 2903 is the device to use since it provides for partitioning via the /OE Output Enable signal. The 2932 lacks the flexibility of the /IEN (instruction enable) and RE (register input enable) functions, and is not recommended for both system (board) functional design and testability reasons. Testing of 2901 series boards can be accomplished with access to control points (primarily /OE lines).

Recent bit slice advances have introduced the 29300 and 29C300 (CMOS) chips but incorporating some major 2900 bit slice family differences, i.e., each CPU has a fixed 32-bit data bus and the micro instruction sets are optimized for easy compiler writing. Even though these CPUs are not RISC they can execute one instruction per clock cycle (but the RISC processors are easier to use). Another recent 16-bit SLICE processor is the Word SLICE GP numeric microprocessor by ADI.

These bit slice devices have very specific uses and covering their testability here goes beyond the scope of this handbook. (Remember to get control of all I/O pins.)

9.8 Single Chip/Embedded Microcontrollers.

Embedded single chip controllers are already controlling everything from automatic home appliances to super tankers and space craft. Independent researchers have predicted that the 16- and 32-bit embedded processor market wi'l become the largest segment with business in the micro-device industry for the 1990s (exceeding $5 billion dollars by 1993).

Recent market trends have shown a marked shift in use of 16 and 32 bit microprocessors from programmable to embedded system applications, with a 1992 ꝑrojected 32-bit embedded microprocessor at 10 million units.

This market is showing such growth potential that many manufacturers of 32-bit RISC technology are reorientating their plan to serve this market. (Intel, for instance, moved its 80960 RISC microprocessor from competition with CISC microprocessors to the embedded control market instead).

Present day embedded controllers often need to accomplish their tasks in real time. The parallel processing and RISC technology now utilized rivals anything found in the latest workstations.

One problem is that embedded controllers are usually not reprogrammable once installed in a system. Problems in a computer can cause temporary aggravation but problems in an embedded controller can destroy end user systems.

With these factors in mind, the following list gives an outline of some of the main characteristics needed by embedded controllers.

- Rapid interrupt handling
- Concurrent handling of multiple functions
- Fault tolerance
- Redundancy requirements
- Low power consumption/heat dissipation
- Compact size
- Ability to handle many I/O lines
- Efficient memory utilization

9.8.1 The 8048 Microprocessor Family. This family of devices is more aptly named a family of microcomputers, rather than microprocessors, since each device contains its own ROM and scratch pad memory. This means that a single chip can operate as a complete system for simple applications.

The devices in this family and the pin-outs are depicted in figure 9-40.

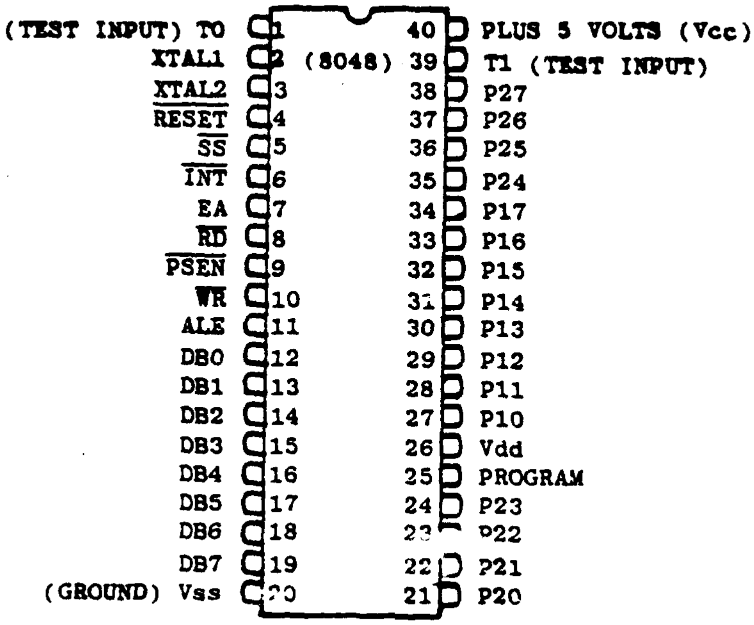


Figure 9-40. 8048 Family (DIP)

Typical testing procedure for these devices includes initial reset, verification of internal ROM, initialization/loading of scratch pad memory and, finally, allowing the processor to execute the testing patterns.

Testability considerations are again aimed at control and visibility.

Control points required include:

• TO,	test input
• EA,	external program memory access line
• /SS,	single step control line
• /INT,	interrupt request
• /RESET,	chip RESET line

Visibility points required include:

• ALE,	address latch enable (SYNC) line
• /RD,	data memory read control
• /WR,	data memory write control
• /PSEN,	external memory read control line

Since these devices contain on-chip clocks, the same technique mentioned for the 8085A should be employed for clock control, unless the ATE system can synchronize with the crystal or RC network and keep up with the microcomputer. Strobe synchronization should be referenced to the ALE line.

After the reset operation, the TO line should be used to verify internal memory on the device. The EA line can be used to force the device into the "DEBUG" mode, where it must access external program memory; in this case, an ATE system.

These devices also have a single step mode, to allow relatively straight forward interface requirements and make testing on I/O rate test systems easier. A typical circuit configuration which allows the ATE system to control and make use of the single stepping feature is shown in figure 9-41.

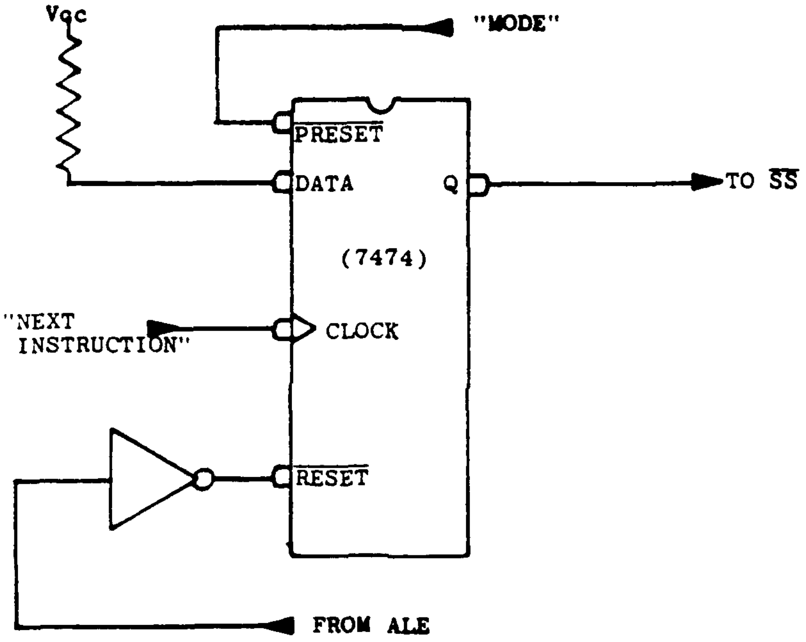


Figure 9-41. Single Step Control Circuit for the 8048

In this circuit, the line marked MODE, which comes from the ATE system, determines whether the processor will run at speed or single step, instruction by instruction. With a logic 0 applied to the mode input, the processor will run at speed. A logic 1 applied to this input will force the single step mode, and each instruction will execute on activation of the next instruction line, which also comes from the tester.

This suggested circuit can be easily added to a PC board under test; it may also be used by the designer to aid in debugging using standard development tools. It is a plus for both the test engineer and the design engineer.

9.8.2 The 68070 Embedded 32-Bit Microprocessor. The Philips/Signetics SCC 68070 CMOS microprocessor reduces system cost and power consumption by combining the power of a 68000 compatible CPU with advanced and standard peripherals integrated on a single chip. See figure 9-42.

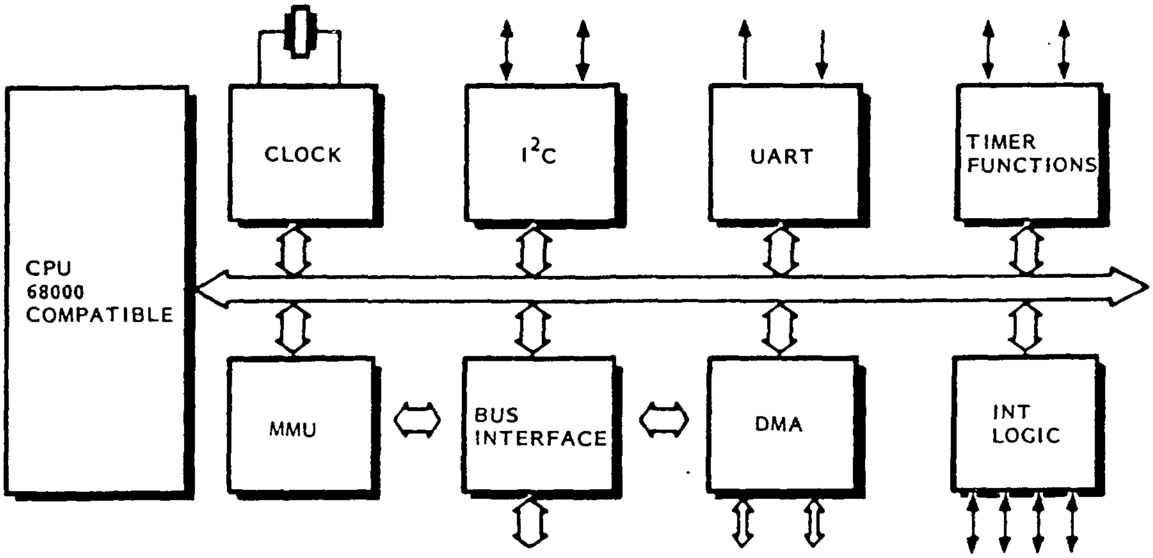


Figure 9-42. Simplified Block Diagram of 68070

The 84-pin PLCC housing the 68070 has a power consumption (at 20 MHz input frequency) of 400 mW maximum and 200 mW typical.

The internal 32-bit bus links a Memory Management Unit (MMU), 2-channel Direct memory Access controller (DMW), UART serial interface, IIC bus serial interface, and a 16-bit Counter/Timer with the 16/32 bit CPU. Hardware connections between on-chip peripherals and the external bus are simplified by using standard signal connections and maintaining full support of the 68000 instruction set. 68070 op code is downward compatible with 68000/008/010 and user software operates unaltered on the 68000 processors.

As of this writing the actual block diagrams and pin information did not arrive in time to create a detailed testability analysis for this chip, but controllability and visibility is needed for all chip I/O.

9.8.3 Intel 80960CA (Super Scalar). Intel's 1st generation 80960 RISC 32 bit microprocessor executing one instruction per clock cycle, have recently been eclipsed by the 80960 CA Super Scalar microprocessor (Oct 1989).

The 80960 CA has a 4-6 times increased overall performance over the original 80960 and can execute up to 4 separate instructions per clock cycle. This is accomplished largely through internal architecture but also increasing the system clock speed by only 1.3 times.

Intel calls this nonlinear performance increase (with respect to the clock rate) SUPER SCALAR performance.

With 3 parallel internal pipelines, the 80960CA averages 66 MIPS at 33 MHz. Although its on-chip cache is small, it is arranged particularly well to suit embedded control.

The i960 series and all of its versions were designed specifically for embedded control applications.

The 80960MC chip family was recently chosen as one of two 32- bit instruction set standards by the Military to succeed the 16-bit 1750A military standard.

The most conspicuous departure of the 80960CA from RISC design is its use of microcode. This removes burden of memory delays and procedural overhead. Also, the 80960CA has built in hardware with break points to simplify software debugging.

On-chip self-test features aid troubleshooting and system maintenance. Built in testability greatly aids in chip testing of this complex design. Figure 9-43 and 9-44, give an overview of this chip's capabilities.

9.8.3.1 Debug Features. The 80960MC has built-in debug capabilities. There are two types of break points and six different trace modes. The debug features are controlled by two internal 32-bit registers, the Process-Controls Word and the Trace-Controls Word. By setting bits in these control words, a software debug monitor can closely control how the processor responds during program execution.

The 80960MC has both hardware and software break points. It provides two hardware break point registers on-chip which can be set by a special command to any value. When the instruction pointer matches the value in one of the break point registers, the break point fires, and a break point handling routine is called automatically.

- High-Performance Embedded Architecture
  - — 20 MIPS Burst Execution at 20 MHz
  - — 7.5 MIPS* Sustained Execution at 20 MHz
- On-Chip Floating-Point Unit
  - — Supports IEEE 754 Floating-Point Standard
  - — Full Transcendental Support
  - — Four 80-Bit Registers
  - — 4 Million Whetstones/Second at 20 MHz
- 512-Byte On-Chip Instruction Cache
  - — Direct Mapped
  - — Parallel Load/Decode for Uncached Instructions
- Multiple Register Sets
  - — Sixteen Global 32-Bit Registers
  - — Sixteen Local 32-Bit Registers
  - — Four Local Register Sets Stored On-Chip (Sixteen 32-Bit Registers per Set)
  - — Register Scoreboarding
- On-Chip Memory Management Unit
  - — 4 Gigabyte Virtual Address Space per Task
  - — 4 Kbyte Pages with Supervisor/User Protection
- Built-In Interrupt Controller
  - — 32 Priority Levels
  - — 248 Vectors
  - — Supports M8259A
- Easy to Use, High Bandwidth 32-Bit Bus
  - — 43 MBytes/s Burst
  - — Up to 16-Bytes Transferred per Burst
- Multitasking and Multiprocessor Support
  - — Automatic Task Dispatching
  - — Prioritized Task Queues
- Advanced Package Technology
  - — 132 Lead Ceramic Pin Grid Array
  - — 164 Lead Ceramic Quad Flatpack
- Military Temperature Range
  - — − 55°C to + 125°C (T_C)

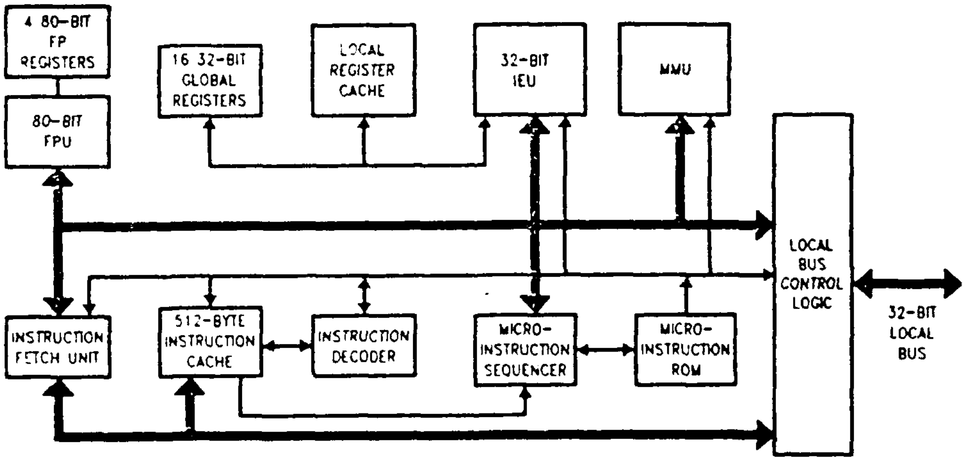


Figure 9-43. Block Diagram of 80960MC
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

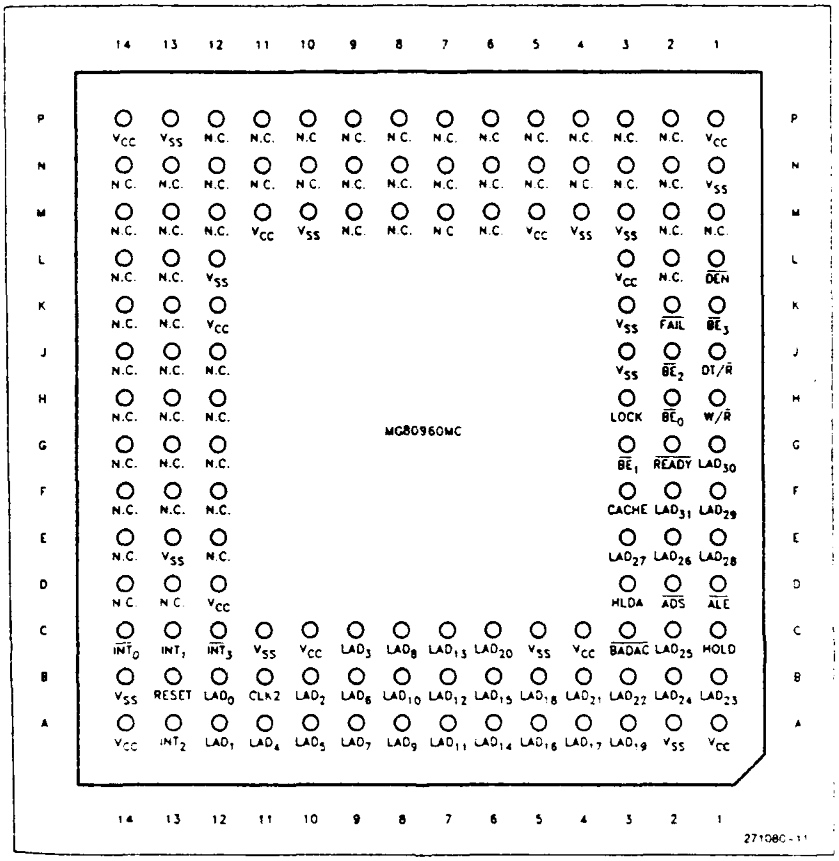

14 13 12 11 10 9 8 7 6 5 4 3 2 1
P V_{CC} V_{SS} N.C. N.C. N.C N.C. N.C. N.C. N.C N.C. N.C. N.C. N.C. V_{CC} P
N N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N.C. V_{SS} N
M N.C. N.C. N.C. V_{CC} V_{SS} N.C. N.C. N.C N.C. V_{CC} V_{SS} V_{SS} N.C. N.C. M
L N.C. N.C. V_{SS} V_{CC} N.C. $\overline{DEN}$ L
K N.C. N.C. V_{CC} V_{SS} $\overline{FAIL}$ $\overline{BE}_3$ K
J N.C. N.C. N.C. V_{SS} $\overline{BE}_2$ $DT/\overline{R}$ J
H N.C. N.C. N.C. LOCK $\overline{BE}_0$ $W/\overline{R}$ H
MG80960MC
G N.C. N.C. N.C. $\overline{BE}_1$ $\overline{READY}$ LAD_{30} G
F N.C. N.C. N.C. CACHE LAD_{31} LAD_{29} F
E N.C. V_{SS} N.C. LAD_{27} LAD_{26} LAD_{28} E
D N.C. N.C. V_{CC} HLDA $\overline{ADS}$ $\overline{ALE}$ D
C $\overline{INT}_0$ INT_1 $\overline{INT}_3$ V_{SS} V_{CC} LAD_3 LAD_8 LAD_{13} LAD_{20} V_{SS} V_{CC} $\overline{BADAC}$ LAD_{25} HOLD C
B V_{SS} RESET LAD_0 CLK2 LAD_2 LAD_6 LAD_{10} LAD_{12} LAD_{15} LAD_{18} LAD_{21} LAD_{22} LAD_{24} LAD_{23} B
A V_{CC} INT_2 LAD_1 LAD_4 LAD_5 LAD_7 LAD_9 LAD_{11} LAD_{14} LAD_{16} LAD_{17} LAD_{19} V_{SS} V_{CC} A
14 13 12 11 10 9 8 7 6 5 4 3 2 1
271080-11

Figure 9-44. Pin Outs for 80960MC
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

The 80960MC also provides software break points through the use of two instructions, MARK and FMARK. These instructions can be placed at any point in a program and cause the processor to halt execution at that point and call the break point handling routine. The break point mechanism is easy to use and provides a powerful debugging tool.

Tracing is available for instructions (single-step execution), calls and returns, and branching. Each different type of trace may be enabled separately by a special debug instruction. In each case, the 80960MC executes the instruction first and then calls a trace handling routine (usually part of a software debug monitor). Further program execution is halted until the trace routine is completed, and Instruction execution resumes at the next instruction. The 80960MCs tracing mechanisms, (implemented completely in hardware), greatly simplify the task of testing and debugging software.

9.8.3.2 Fault Detection. The 80960MC has an automatic mechanism to handle faults. There are ten fault types including trace, arithmetic, and floating-point faults. When the processor detects a fault, it automatically calls the appropriate fault handling routine and saves the current instruction pointer and necessary state information to make efficient recovery possible. The processor posts diagnostic information on the type of fault to a Fault Record like interrupt handling routines, fault handling routines are written to meet the needs of a specific application and are included as part of the operating system or kernel.

For each of the ten fault types, there are numerous subtypes that provide specific information about a fault. For example, a floating-point fault may have its subtype set to an Overflow or Zero-Divide fault. The fault handler can use this specific information to respond correctly to the fault.

9.8.3.3 Fault Tolerance. The term fault tolerance refers to the ability of a system to detect errors in its own operation and then take self-corrective action to prevent errors from corrupting data or leading to wrong actions. Many fault- tolerant systems rely on software to do checking and provide recovery; the 80960MC's fault-tolerant mechanisms are based exclusively on hardware mechanisms and the replication of VLSI components and buses.

When the 80960MC processor is used with Intel's M82965 Bus Extension Unit, systems can easily be built that tolerate the failure of any single component or bus and continue to operate correctly.

Each 80960MC processor is able to detect hardware errors automatically because of a capability known as Functional Redundancy Checking (FRC), so called because a second or redundant processor checks the operations of the first or master processor. FRC provides the low-level hardware support upon which hardware fault-tolerant modules are constructed.

While FRC can be used alone to provide automatic error detection, a completely fault-tolerant system must also reconfigure itself, replacing the set of failed components with another pair that is still working.

In order to do so, the M82965 Bus Extension Unit enables two pairs of master/checker components to be combined to form primary and shadow processors in a configuration known as Quad Modular Redundancy (QMR).

Each processor module in a QMR system is paired with another self-checking module which operates in lock step (see figure 9-45). The mechanism is known as module shadowing because a shadow is ready to fill in if the primary fails (or vice versa). Fault detection and recovery occur automatically without the intervention of either application or operating system software. When a fault is detected, the faulty pair is automatically disabled and the remaining pair takes over. Thus the operating system is notified, a failure has occurred.

It is essential that the fault tolerant architecture can be controlled in such a way as to check just the operation of the processors individually. Disabling the processor modules independently to simulate a fault is the simplest method to partition a fault tolerant structure.

Note: Section 9.8.3 was taken with the kind permission from Intel, from the Intel 16/32 Embedded Processor Data Book.

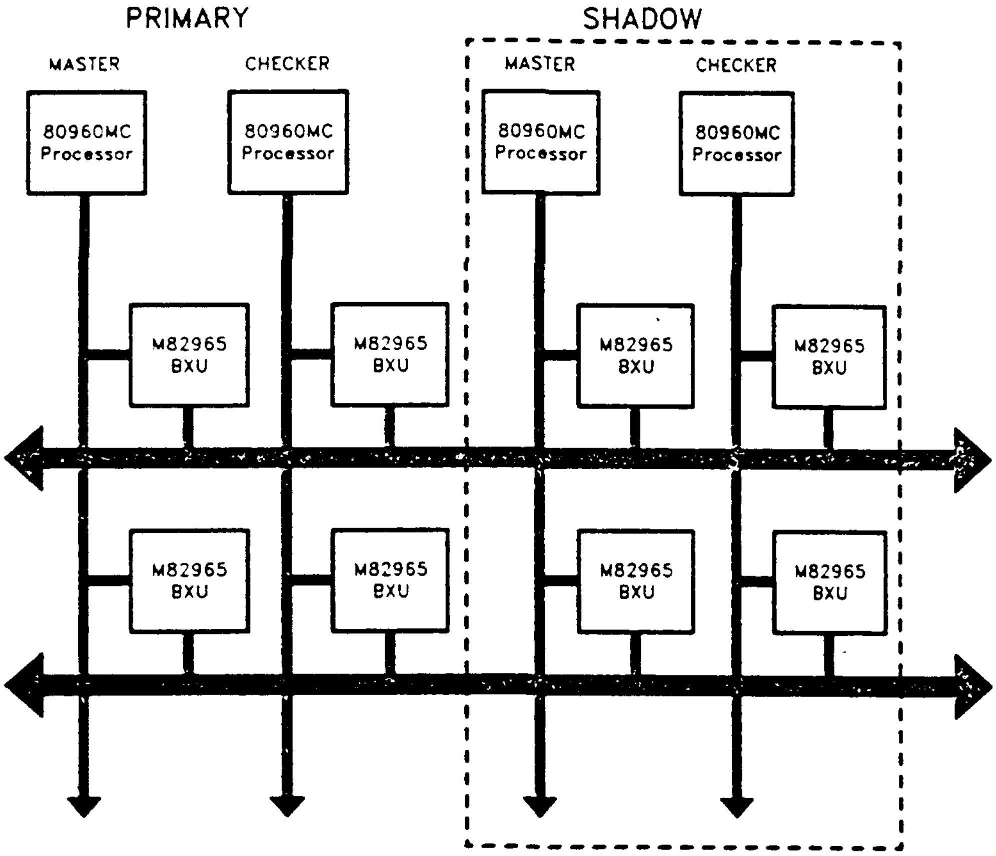


Figure 9-45. Sample for Fault Tolerant System
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

9.8.3.4 Testability Control/Visibility Points

- Control lines include:

  For 80960MC: CLKZ, /READY, /LOCK, HLDAR, /BADAC, RESET,HOLD, IAC, INTO, INT1, INT2, INTR, INT3, /INTA

- Visibility lines or test points include:

  For 80960MC: /ALE, /ADS, W/(not)R, DT/(not)R, /DEN, /LOCK, BE3-BE0, HLDA HOLDR, CACHE, /FAILURE, /INT3, /INTA

9.9 Digital Signal Processors (DSP) and Others.

DSPs are used for large computational chores that bog down conventional microprocessors. Early DSP applications were relegated to the military and very high end array processing.

With emphasis on performance rather then price; they were set into two main groups.

1. Algorithm specific (special function) DSPs
2. General purpose DSPs
    - Integer DSPs
    - Floating point DSPs

Presently, as conventional RISC chips contirue to mature there is less and less difference between DSP, RISC, CISC, and microcontrollers.

General purpose DSPs that are Floating point chips are far easier to program and require fewer support chips to integrate them into a system even though they are initially more expensive than Fixed point or integer chips.

9.9.1 Intel 80860 64-Bit RISC Microprocessor. One of the most interesting chips on the market today is the 80860 64-bit RISC micrcprocessor used for DSP. It has two distinct processing units on board, one handles integer generation, the other, floating point and graphics operations. It can achieve 40 integer MIPS at 40 MHz (50 MHz in peak performance) and 80 single precision mega flops.

With its 64-bit wide bus it incorporates most of the new VLIW (very long instruction word) architecture. For testability, the 80860 incorporates boundary scan (section 11), one of the latest ideas in digital testing techniques. See section 9.9.1.1 on i860 testability.

The i860 was designed to give balanced performance across integers, floating point, and 3D graphics operation. 33 and 40 MHz samples are available presently. The i860 is designed to run UNIX but not 80386 software. Figure 9-46, 9-47, and 9-48 give information presently available on the i860 from Intel (1990).

9.9.1.1 Testability. The i860 microprocessor has a boundary scan mode that may be used in component- or board-level testing to test the signal traces leading to and from the i860 microprocessor. Boundary scan mode provides a simple serial interface that makes it possible to test all signal traces with only a few connections to CLK, BSCN, SCAN, SHI, BREQ, RESET, and HOLD.

The pins BSCN and SCAN control the boundary scan mode (refer to figure 9-48). When BSCN is asserted, the i860 microprocessor enters boundary scan mode on the next rising clock edge. Boundary scan mode can be activated even while RESET is active. When BSCN is negated while in boundary scan mode, the i860 microprocessor leaves boundary can mode on the next rising clock edge. After leaving boundary scan mode, the internal state is undefined; therefore, RESET should be asserted. Test mode selection is shown in figure 9-49.

- **Parallel Architecture that Supports Up to Three Operations per Clock**
  - **— One Integer or Control Instruction per Clock**
  - **— Up to Two Floating-Point Results per Clock**
- **High Performance Design**
  - **— 33.3/40 MHz Clock Rates**
  - **— 80 Peak Single Precision MFLOPs**
  - **— 60 Peak Double Precision MFLOPs**
  - **— 64-Bit External Data Bus**
  - **— 64-Bit Internal Instruction Cache Bus**
  - **— 128-Bit Internal Data Cache Bus**
- **High Level of Integration on One Chip**
  - **— 32-Bit Integer and Control Unit**
  - **— 32/64-Bit Pipelined Floating-Point Adder and Multiplier Units**
  - **— 64-Bit 3-D Graphics Unit**
  - **— Paging Unit with Translation Lookaside Buffer**
  - **— 4 Kbyte Instruction Cache**
  - **— 8 Kbyte Data Cache**
- **Compatible with Industry Standards**
  - **— ANSI/IEEE Standard 754-1985 for Binary Floating-Point Arithmetic**
  - **— 386™/i486™ Microprocessor Data Formats and Page Table Entries**
  - **— JEDEC 168-pin Ceramic Pin Grid Array Package (see *Packaging Outlines and Dimensions*, order # 231369)**
- ***Easy to Use***
  - **— On-Chip Debug Register**
  - **— Assembler, Linker, Simulator, Debugger, C and FORTRAN Compilers, FORTRAN Vectorizer, *Scalar and Vector Math Libraries* for both OS/2* and UNIX* Environments**

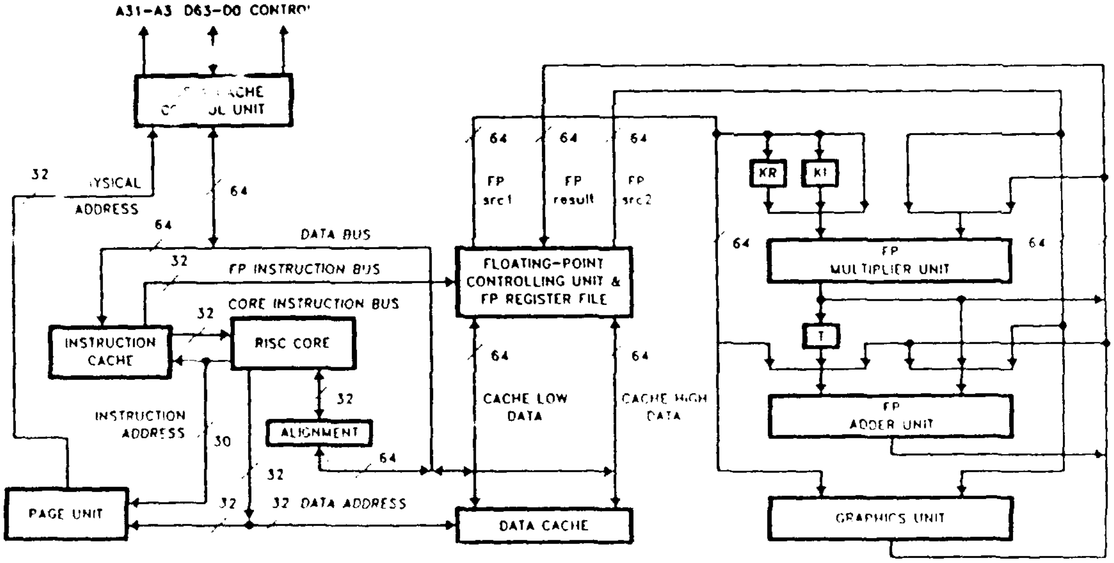
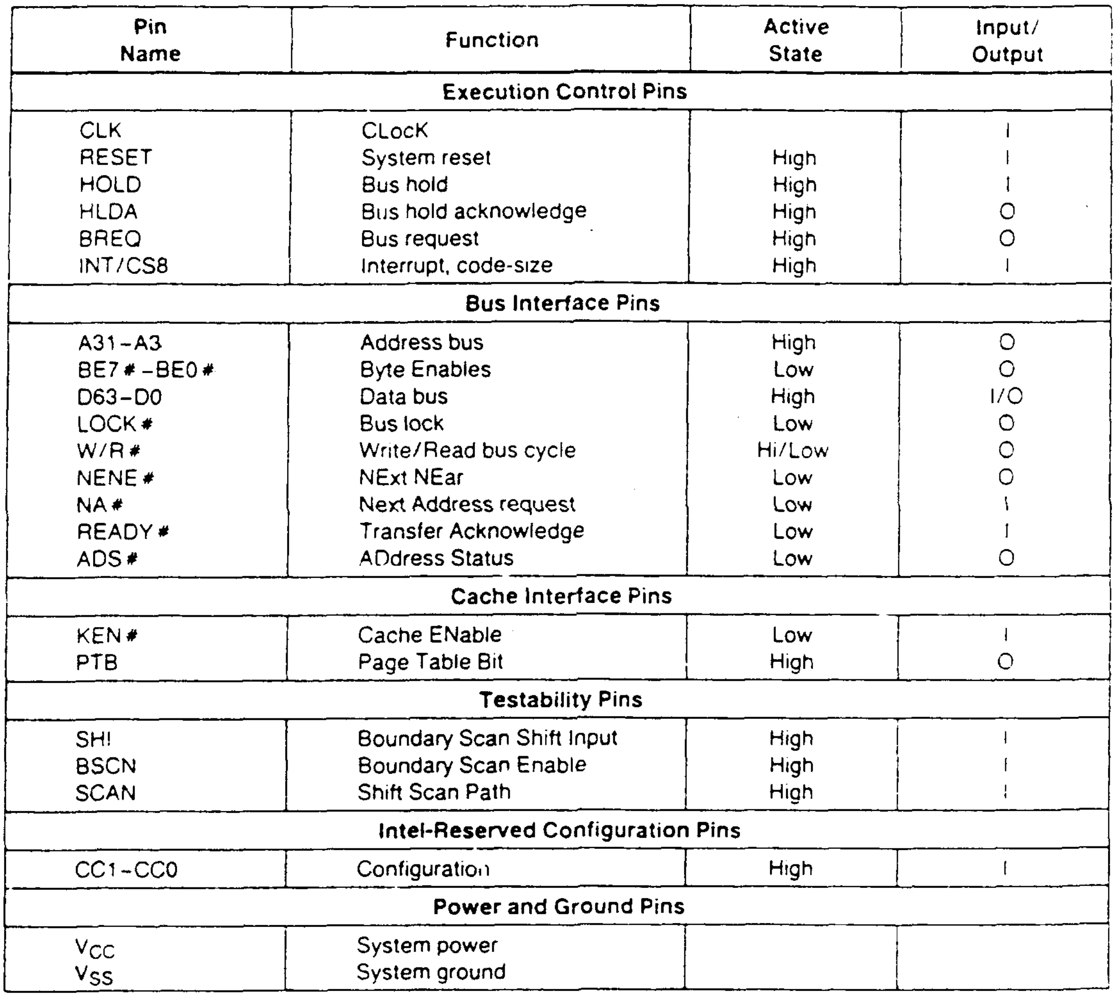


Figure 9-46. i860 Block Diagram
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)



Pin Name	Function	Active State	Input/ Output
Execution Control Pins			
CLK	CLocK		I
RESET	System reset	High	I
HOLD	Bus hold	High	I
HLDA	Bus hold acknowledge	High	O
BREQ	Bus request	High	O
INT/CS8	Interrupt, code-size	High	I
Bus Interface Pins			
A31-A3	Address bus	High	O
BE7#-BE0#	Byte Enables	Low	O
D63-D0	Data bus	High	I/O
LOCK#	Bus lock	Low	O
W/R#	Write/Read bus cycle	Hi/Low	O
NENE#	NExt NEar	Low	O
NA#	Next Address request	Low	I
READY#	Transfer Acknowledge	Low	I
ADS#	ADdress Status	Low	O
Cache Interface Pins			
KEN#	Cache ENable	Low	I
PTB	Page Table Bit	High	O
Testability Pins			
SHI	Boundary Scan Shift Input	High	I
BSCN	Boundary Scan Enable	High	I
SCAN	Shift Scan Path	High	I
Intel-Reserved Configuration Pins			
CC1-CC0	Configuration	High	I
Power and Ground Pins			
V_{CC}	System power		
V_{SS}	System ground		

Figure 9-47. i860 Signal Table
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

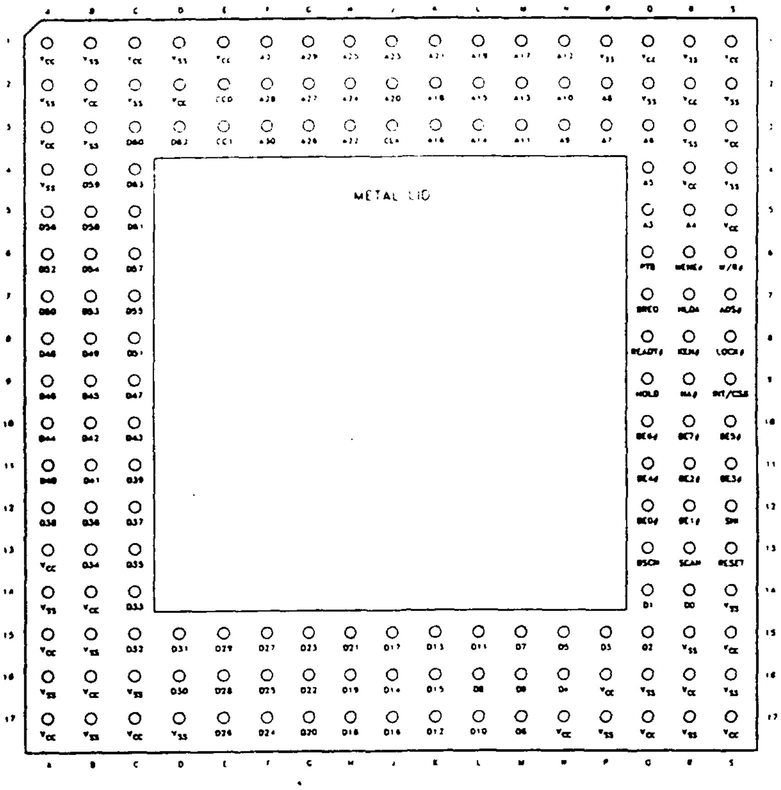
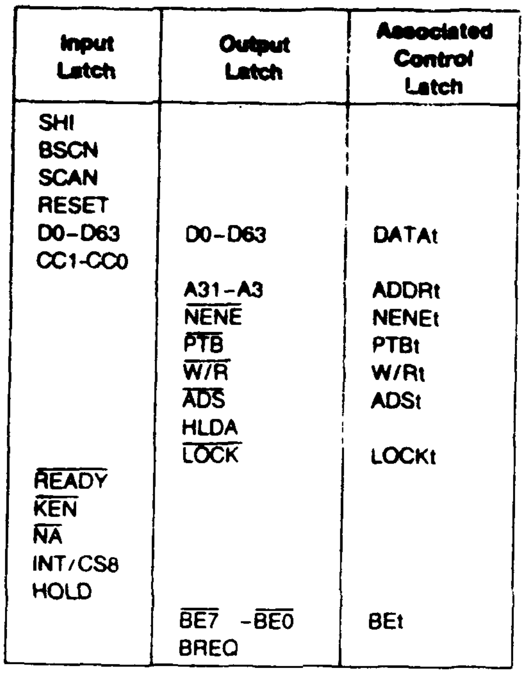


Figure 9-48. i860 Pin Configuration
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

BSCN	SCAN	Testability Mode
LO	LO	No testability mode selected
LO	HI	(Reserved for Intel)
HI	LO	Boundary scan mode, normal
HI	HI	Boundary scan mode, shift SHI as input; BREQ as output

Figure 9-49. Test Mode Selection
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

For testing purposes, each signal pin has associated with it an internal latch. Figure 9-50 identifies these latches by name and classifies them as input, output, or control. The input and output latches carry the name of the corresponding pins.



Input Latch	Output Latch	Associated Control Latch
SHI		
BSCN		
SCAN		
RESET		
D0-D63	D0-D63	DATAt
CC1-CC0		
	A31-A3	ADDRt
	$\overline{\text{NENE}}$	NENEt
	$\overline{\text{PTB}}$	PTBt
	$\overline{\text{W/R}}$	W/Rt
	$\overline{\text{ADS}}$	ADSt
	HLDA	
	$\overline{\text{LOCK}}$	LOCKt
$\overline{\text{READY}}$		
$\overline{\text{KEN}}$		
$\overline{\text{NA}}$		
INT/CS8		
HOLD		
	$\overline{\text{BE7}}$ -$\overline{\text{BE0}}$	BEt
	BREQ	

Figure 9-50. Test Mode Latches
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

Within boundary scan mode the i860 microprocessor operates in one of two submodes: normal mode or shift mode, depending on the value of the SCAN input. A typical test sequence is:

1. Enter shift mode to assign values to the latches that correspond with the pins.
2. Enter normal mode. In normal mode the i860 microprocessor transfers the latched values to the output and latches the values that are being driven onto the input pins.
3. Re-enter shift mode to read the new values of the input pins.

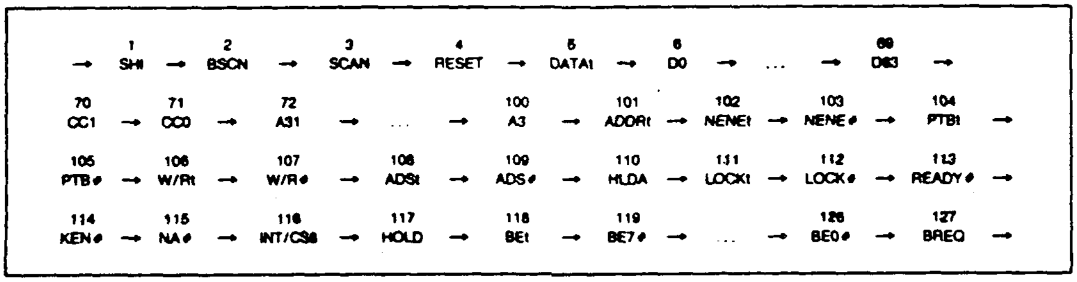
9.9.1.2 Normal Mode. When SCAN is de-asserted, the normal mode is selected. For each input pin (RESET, HOLD, INT/CS8, /NA, /READY, /KEN, SHI, BSCN, SCAN, CC1, and CC0), the corresponding latch is loaded with the value that is being driven onto the pin.

The tri-state output pins (A31-A3, /BE7-/BE0, W/(not)R, /NENE, /ADS, /LOCK, and PTB) are enabled by the control latches ADDRt (for A31-A3), BEt, W/Rt, NENEt, LOCKt, and PTBt. If a control latch is set, the corresponding output latches drive their output pins; otherwise the pins are not driven.

The I/O pins (D63-D0) are enabled by the control latch. DATAt, which is similar to the other control latches. In addition, when DATAt is not set, the data pins are treated as input pins and their values are latched.

9.9.1.3 Shift Mode. Asserting SCAN selects the shift mode and the pins are organized into a boundary scan chain. The scan chain is configured as a shift register and shifted on the rising edge of CLK. The SHI pin is connected to the input of one end of the boundary scan chain. The value of the most significant bit of the scan chain is output on the BREQ pin. To avoid glitches while the values are being shifted along the chain, the tester should assert both the RESET and HOLD pins. Then all tri-state outputs are disabled. The order of the pins within the chain is shown in figure 9-51.

Note: This is not a full implementation of IEEE STD 1149.1 as device does not use a Test Access Port (TAP) as defined in the standard.



→ 1 SHI → 2 BSCN → 3 SCAN → 4 RESET → 5 DATAt → 6 D0 → ... → 69 D63 →

70 CC1 → 71 CC0 → 72 A31 → ... → 100 A3 → 101 ADDRt → 102 NENEt → 103 NENE# → 104 PTBt →

105 PTB# → 106 W/Rt → 107 W/R# → 108 ADSt → 109 ADS# → 110 HLDA → 111 LOCKt → 112 LOCK# → 113 READY# →

114 KEN# → 115 NA# → 116 INT/CS8 → 117 HOLD → 118 BEt → 119 BE7# → ... → 126 BE0# → 127 BREQ →

Figure 9-51. Order of Boundary Scan Chain
(reprinted by permission of Intel Corporation, Copyright/Intel Corporation 1989.)

A tester causes entry into this mode for one of two purposes:

1. To assign values to output latches to be driven onto output pins upon subsequent entry into normal mode.

2. To read the values of input pins previously latched in normal mode.

NOTE: All i860 testability documentation, figures, etc., were taken from Intel 1990 data books courtesy of Intel.

9.9.1.4 Testability Control/Visibility Points.

- Control lines include:

  For 80860: CLK, RESET, HOLD, INT/CS8, /NA, /READY, /KEN, SHI BSCAN, SCAN, CC1-CC0.

- Visibility lines or test points include:

  For 80860: HLDA, BREQ, /BE7, /BE0, /LOCK, W/(not)R, /NENE#, /ADS, PTB.

Although the 80860 has a boundary scan path, it does not fully implement the IEEE 1149.1 standard and it is recommended that the above control/visibility points are used for additional testing purposes.

9.10 Future Processors (General).

In 1989 Intel predicted that "by the year 2000, Microprocessors will include 50 million transistors, on a one inch square die incorporating multiple processors with a total performance speed of 2000 million instructions per second (Mips) running at two hundred and fifty megahertz.

The trend for past microprocessors was to solve the next generations bottlenecks by integrating more functions on a chip. This trend is expected to continue. A good example is the recently released 80486 which besides the 80386 microprocessor also includes the 80387 and several other once separate chips on a single chip. Intel believes that no matter how radical the architectural departures of future microprocessors, they will remain compatible with todays most popular microprocessors. (They should know, as of this writing they have the 80586, the 80686, and the 80786 in various stages of development).

9.10.1 Testability of Future Processors. Can we test 50 million transistor chips in a reasonable length of time? The most advanced present day microprocessors have shown (with 1-2 million transistors on a chip) that without Built-In-Self-Test (BIST) of some form, it would be impossible.

The present trend of including BIST in some form (such as the 68030 and 40, the Intel 80486, etc) will continue as promised by the manufacturers.

Changes on the horizon include microprocessor system power supplies to move from the present 5 volts to 3.3.volts or even 2.5 volts by the year 2000.

These new microprocessor will run very "hot" and will need very elaborate cooling schemes which may make physical accessibility much more difficult then at the present.

At these speeds all present ATE equipment could be quickly obsoleted and whole new technologies of packaging/interconnect test adapters/ and drive pin electronics will have to be developed.

The following section will give an overview of what is presently on the microprocessor manufactures drawing boards to be released in the next few years.

9.10.2 Specific Future Processors. The DSP processor 80860 is one of the first second generation microprocessors with 64-bit wide I/O, although a 128-bit processor is predicted for the 1990s. (A 128-bit processor can access 3.402 X 10^{38} bytes).

Within 10 years 64-bit microprocessors will be common place in PCs and be able to access 1.84 x 10E-19 memory bits.

These immensely complex chips will all have to have extensive self-test capabilities and incorporate structurcu design for test techniques like boundary scan or they will make a test engineers life a nightmare.

One of the newest chip sets on the market is the IBM AMERICA Super Scalar (RISC) processor which can execute 5 (five!) instructions in one clock cycle. The 9 chip set has 6.9 million transistors, packaged in nine 300 pin ceramic grid arrays consuming 4 watts each. The set uses CMOS ASICs. This chip set has propelled IBM to the lead in computer architectures.

No word on chip testability as yet but it is assumed the set includes boundary scan of some sort.

Other future development plans now on the drawing boards:

1. Norway's Dolphin Server Technology Inc. plans a Motorola 88000 RISC microprocessor in ECL.

   Expected performance:

   a. 1000 MIPS at 125 MHz

   b. Execute 8 instructions in parallel

   c. CPU alone incorporates 13 ECL gate arrays

Note: Original CMOS 88K is a three chip set (CPU and two MMUs). Total implementation by Dolphin will be two dozen ECL gate arrays by 1992.

   (Data General/Motorola team working on a 4 gate array 88K ECL version capable of only one instruction per clock cycle.).

2. Intergraph's future CLIPPERS beyond C300 include:

   a. C400 (27 to 34 MIPS), CMOS, 40-50 MHz.

   b. C500 (40 to 47 MIPS), 60-70 MHz.

   c. ECL CLIPPER E100 70 MIPS at 100 MHz.

3. Cypress Semiconductor Corp. is planning a SPARC SERVER 490:

   a. Based on HEMT (TRANSISTOR) switching technology recently announced by Hughes Aircraft company at 250 Giga Hertz without cooling.

4. Sharp Corporation (Japan) is building a 3 dimensional microprocessor chip. It passes information vertically between 3 levels, eliminating need for synchronous clocks.

   Testability of these new microprocessor technologies will become a challenge in the very near future.

9.11 Microprocessor Support Chip Testability.

The 16 bit/32 bit microprocessor support chip market has grown right along with th. microprocessor market.itself. Many of the support chips were adapted from the original eight bit microprocessor support chip hv only widening their data lines (but many are also new designs).

This section provides an outline of testability measurements for 15 of the most popular 680XO microprocessor families support chips in a table (see table 9-3). This will give the designer/test engineer an idea of the type of lines that need to be controlled/and or made visible. Probably the most difficult testability task in fault isolation techniques is to find an intermittent and where on a bus it actually occurs. Bus Driver/Transceiver control allows for quickest isolation. For additional control, some gates can be added to any input lines where necessary.

It should be noted that although not shown, signal control of address lines and visibility of data lines is essential.

Table 9-4 shows how the Motorola chips relate to similar chips made by Intel and Zilog.

Table 9-3. Support Chip Testability Chart

#	Support Chip	Chip Name	Testability Requirements		Comments
			Control Points	Visibility Points	
1	68120	Inteligent Peripheral Controller	/RESET, /CS, CLK, TIMERIN	/DTACK, TIMEROUT	-
2	68230	Parallel Interface Timer (PI/T)	CLK, PC0:7, RS1:5, H1:4, /RESET, /CS	/DTACK (Bidirectional lines shown in control column)	An on-chip square wave generator can be controlled by the clock input. The asynchronous timer and I/O ports usually present testability problems.
3	68440	Dual Direct Memory Access Controller (DDMA)	/CS, /BEC0:2 /DONE	/DBEN, /DDIR, /ACK1:4, /DTC	This chip has no "reset" line so other lines need to perform this task.
4	68450	Dual Direct Memory Access Controller (DDMA)	"	"	Same as 68440. These chips operate independently and need to be well partitioned from the rest of the circuit.
5	68451	Memory Management Unit (MMU)	/CS, /RESET, /ED, MODE, /MAS, /HAD, /IRQ, /FAULT	/ANY, ALL	/MAS, /ED, and ALL signals require pullup resistors.
6	68454	Inteligent Multiple Disk Controller IMDC	/RES, /BG, /CS	EN0, EN1, /DTRACK, LOCAL, DDIR, OWN	-
7	68465	Floppy Disk Controller FDC	/RESET, /CS, TIMERIN, ACK, /DONE	/DTACK, TIMEROUT	-
8	68563	Multiple Protocall Communications Controller-II (MPCC-II)	/RESET, /CS, EXTAL	/DTACK, BCLK	-
9	68562	Dual Universal Serial Comm. Controller (DUSCC	/RESET, /CS, X1/CLK, X2/IDC	/DTACK	-
10	68590	Local Area Network Controller (LANCE)	/RESET, /CE, RS, /HLDA, /READY	ALE/(not)AS, HOLD/(not)BUSRO	-
11	68562	Multiple Protocal Comm. Controller (MPCC)	DREN, RxC, TxC, MM, RGET, CE	SYNC/FLAG	MM line can be used for loop-back Testing chip off-line (TxS0 to RxSI and TxC to RxC).
12	68563	Polynomial Generator Checker (PGC)	/CE0 (or /CE1), A0, A1	/INT	There is no RESET line. Use software to set internal registers to a known state.
13	68661	Enhanced Programmable Comm. Interface (EPCI)	RESET, /CE, BRCLK, /DCD, /CTS, /DSR	/TxRDY, /RxDSY, (not)TxC/SYNC, (not)RxC/BKDET, TxEMT/(not)DSCHG	-
14	68681	Dual Universal Async Rec/Xmtr (DUART)	RxDA, RxDB, CLK RS1:4, /RGET, /CS	TxDA, TxDB	As with all UARTs, a loop-back test is the best way of testing this device.
15	68901	Multi-Function Peripheral (MFP)	/RESET, /CS, SI, /IEI, SO, RC, TC	IRQ, /DTACK, and all clock outputs	-

Table 9-4. Support Chip Cross Reference

MOTOROLA PART NO.	MNEMONIC	DESCRIPTION	DESCRIBED FOR TESTABILITY + PARAGRAPH #	INTEL APPROX. EQUIVAL. PART NO.	ZILOG APPROX. EQUIVAL. PART NO.
68120	IPC	Intelligent Peripheral Controller	X	8255A	Z8590/4
68121	IPC-NR	IPC with no ROM	—	—	—
68122	CTC	Cluster Terminal Controller	—	—	Z8430
68153	BIM	Bus Interrupt Module	—	—	—
68172	E-BUSCON	VME Bus Controller	—	—	—
68173	S-BUSCON	VMF Bus Controller	—	—	—
68174	E-BAM	VME Bus Arbitration Module	—	—	—
68200	MCU	Micro-Computer Unit	—	—	—
68230	PVT	Parallel Interface/Timer	X	—	—
68340	DPR	Dual Port Ram	—	—	—
68341	IEEE FP	IEEE Floating Point (Software Package-M68KFPS)	—	—	—
68342	RTE	Real Time Ecsecutive (Software Package)	—	—	—
68343	FFP	Fast Floating Point (Software Package M68KFFP)	—	—	—
68345	FIFO	First In/First Out	—	—	Z8060
68430	DMAI	DMA Interface	—	—	—
68440	DDMA	Dual DMA	X	—	Z8410
68450	DMAC	DMA Controller	X	82258	Z8516
68451	MMU	Memory Management Unit	X	—	Z8010
68452	BAM	Bus Arbitration Module	—	—	—
68454	IMDC	Intelligent Multiple Disk Controller	X	82064	—
68459	DPLL	Disk Phase Locked Loop	—	—	—
68465	FDC	Floppy Disk Controller	X	8271,2 (82072)	Z765A
68485	RMC	Raster Memory Controller	—	—	—
68486	RMI	Raster Memory Interface	—	—	—
68561	MPCC-II	MultiProtocol Communication Controller II	X	—	—
68562	DUSCC	Dual Universal Serial Comm. Controller	X	82530	Z8530
68564	SIO	Serial Input Output	—	8243	Z8440,1,2,4
68590	LANCE	Local Area Network Controller	X	—	—
68605	SDMA	Srelal DMA	—	—	—
68652	MPCC	MultiProtocol Comm. Controller	X	—	—
68653	PGC	Polynomial Generator Checker	X	—	—
68661	EPCI	Enhanced Programmable Comm. Interface	X	—	—
68681	DUART	Dual Universal Async. Receiver/Xmitter	X	—	Z8470
68802	LAN-802.3	Local Area Network (IEEE 802.3 Std.)	—	—	—
68851	PMMU	Paged Memory Mangement Unit	—	—	Z8015
68881	FPCP	Floating Point Co-Processor	—	—	Z8070
68901	MFP	Multifunction Peripheral	X	—	—
68920	MAC	Memory Access Controller	—	8203	Z8516

SECTION 10. MEMORY AND PROGRAMMABLE LOGIC DEVICES

10.0 OVERVIEW.

In the last few years, the memory market has become very complex. In addition to core memory which is still in use, we now have bubble memory, flash memory, hard disk, floppy diskette, digital memory, cache, optical memory, fluid memory, and virtual memory. Each memory type has its own unique testability guidelines. Only the most prominent and commonly used forms of memory will be discussed followed by a discussion of general memory testability techniques.

10.1 General Memory Testability Guidelines.

Memory devices are typically 100% functionally tested (i.e.each memory cell has been exercised to prove it can store and retrieve a "0" and a "1" at least once and is independent of all other cells). Memory testing can be traced back to memories associated with the first computer projects (which predate the transistor). These earlier tests were developed to write known patterns into memory and then read these patterns back for evaluation and comparison. In todays market, there are some types of memories which cannot be tested in this way; such as Programmable Read Only Memory (PROM) devices, where once the fuse is blown, it can no longer be reversed. Other devices such as certain UVE PROMs (ultra-violet erasable PROMs) can only be written and erased a limited number of times (as little as 100) before the device breaks down and becomes useless.

These parts cannot be used for classified data since to erase their data requires at least 100 checkerboard pattern reversals of each memory cell. In the case of Top Secret data, 1000 pattern reversals are needed per bit.

ROMs and PROMs have additional problems in that once they are blown, bits can grow back on a molecular level changing the intended program. Random Access Memory (RAM) devices without protected shielding can have their memories altered by cosmic or nuclear radiation.

Memory ICs have grown tremendously in the amount of bits per chip. As of this writing, we are up to 4 million bits for commercially available Dynamic Random Access Memory (DRAM) and 64 million bits for experimental DRAMs. With such large amounts of memory room available on ICs, the days of hard drive memories will soon be over.

Memories in digital systems must function 100% fault free since any failure could lead eventually to a UUT malfunction which can usually not be tolerated. Therefore, there can be no substitute for "100% testing". A 99.999% average sounds impressive but means that in a 1 Megabit DRAM 10 bits are untested and could be faulty.

10.2 Memory and PLD Testability Techniques and Guidelines.

The following testability techniques and guidelines are grouped by memory device type and Programmable Logic Devices (PLDs).

10.2.1 Memory ICs.

1. Choose totally self checking memory ICs if possible. As devices become larger and larger (i.e., 4 MEG single chip DRAMs), totally self checking circuitry is starting to appear as the only cost effective testability method for these devices.

2. Dynamic RAMs are refreshed using a strobe input every few milliseconds to renew the present state of the memory. Access to this strobe input is essential when testing these devices.

3. On-Board ROMs can be tested by performing a binary addition on all locations within the memory device and comparing it to a known correct value. This test is called a checksum test. The binary sum is referred to as a checksum value and it should be stored in the last two addresses of the memory device.

4. Some older PROMs require two voltages for read out. Avoid the extra complexity and do not use this type of device.

5. Occasionally PROMs may contain "proprietary" information. Without access to the security bit, complete memory readout and testability is impossible. Use of these devices should be avoided or made removable for testing of the remaining circuit through test access to the removed PROM's socket.

6. Electronically Erasable PROM (EEPROM) write-cycle life span can range from 100 times to over one million times depending on the device technology, type, and environment. Before a "long" test cycle begins, information about the devices and their history is important because this device may have a limited lifetime.

7. In the last few years FLASH memories have been introduced. They are the best alternative to using EEPROMs. Flash memories provide electrical reprogramming at a fraction of the EEPROM cost and are much smaller in physical size: Their functionality may be slightly less, but if this can be tolerated. The size reduction of the main circuit will provide more room for test circuitry or other purposes.

8. If a device has a low write-cycle life span, it needs to be socketable so it can be easily removed on failure and can be easily substituted for with an emulator for test.

9. Besides the program information, logic equation, and truth tables being available, the test department needs the manufacturers device specifications, documentation, and application notes, especially for more complex devices.

10. Try to use only memory ICs with maximum timing information available. It is often necessary, since parts are working at faster and faster clock cycles, for test equipment to control the clock lines in very precise timing combinations.

10.2.2 Magnetic Storage Devices.

10.2.2.1 Magnetic Tape. These days magnetic tape serial memory is basically used to back-up or archive large amounts of data. This form was popular up to early 80s but will be replaced by optical memory in the form of Compact Disk (CD) ROMs in the 90s. Testability of magnetic tape depends on the tester that is available to read the information from tape, the tape quality, the tape reader read quality, and the cleanliness of the tape and tape head. Generally this media should be avoided and instead use optical memory (para.10.2.3).

10.2.3 Optical Memory. Write Once Read Many (WORM) CD-ROMs should all be replaced with erasable versions, otherwise, no corrections of faults or memory testing is possible. Four manufacturers: 3M, Sharp, Sony, and Maxtor make interchangeable erasable CD-ROMs using Thermo-Magneto-Optics technology following the International Standards Organization (ISO) which allows for a million alternate read write reversals. Any of these four memory systems should be used for greater testability.

Even more exotic memories are on the horizon, known as holographic memory where information from literally 1000s of CD-ROMs will be stored in a 6 inch cube. Designing this type of memory for testability will present a formidable task requiring lasers and sophisticated electronic equipment.

10.2.4 Core Memory. Memory technology has progressed to the point where core memory is no longer necessary. The US Space Shuttle has recently made plans to replace all core memory with CMOS memory chips. Core is bulky, heavy, fragile, and often difficult to easily access with present day testers (not set up for core). All core memory should be replaced with CMOS memory chips to ease testability of these items with present day testers.

10.2.5 Bubble Memory. Bubble memory (non-volatile, 500 Gs, MTBF = 25 years, full MIL temperature range) has unique testability requirements, but they can be greatly reduced and simplified by implementing 100% manufacturer's source testing.

Bubble me.nory is a magnetic medium which is housed in a mu-metal shield. This shield may not prove adequate and more protection may be necessary from the magnetic fields generated in a typical test environment.

Bubble memory contains 15% spare memory loops. A device may have 15% bad memory loops and still be classified as a good device. If the tester has adequate access to control the bubble memory lines and the applicable software, then the test engineer's task of re-routing the failed memory loops is made easier.

10.2.6 Virtual Memory. Virtual memory is a software technique by which a program can be run that exceeds in size the memory capacity of the computer it is being run on. This is done by running only parts of a large program at a time.

10.2.7 Programmable Logic Devices (PLDs). This category includes Programmable Array Logic (PAL), Programmable Logic Arrays (PLAs), Field Programmable Logic Arrays (FPLAs), GALs, and all other PLD forms.

GALs are Generic Array Logic that can be programmed and reprogrammed to look like any type of common PAL. GALs run on lower power than PALs, therefore they can be used as an alternative to PALs.

General PLD testability techniques include:

1. If illegal states are possible in the memory of a PLD, then a test needs to be created which will access the illegal states to see if they can influence the Circuit Card Assembly (CCA) design such as causing a logic "lock up".

2. Be able to tri-state all PLDs, especially PLDs which are "upstream" from complex devices. Without tri-stating upstream PLDs, it is difficult, if not impossible, to test specific "downstream" memory devices.

   Replacing all 'glue logic' with PLDs will reduce testability problems providing that the PLDs implement tri-state visible outputs.

3. Access to all device memory locations (including spare or unused ones) is desirable for potential use of the spare locations during specific device tests.

4. Oscillators can be "buried" in PLD designs without external access to them provided, thus making these devices almost impossible to test. Dedicated oscillator enable/disable pins need to be designed into the circuitry, or on-board oscillators need to be avoided.

5. Placing a PLD into a feedback loop should be avoided, it can be a messy procedure for testability purposes. It greatly increases the amount of logic in the feedback loop and requires more test vectors to test it.

6. Memory elements created by feedback around a 3-state type combinational output (0,1,high Z) may necessitate the tester and the PLD to be simultaneously active to reliably latch data especially on CMOS parts. Any test made may disturb this "latch loop" and may result in race conditions that produce intermittent failure of good parts! Avoid this by designing the 3-state operation to be independent of memory operation.

7. Identical functioning PLDs from different manufacturers have radically different internal architectures requiring different test programming Software (S/W). If the available tester does not have this S/W available, testing PLDs can be impossible.

8. Beware of failures to PLDs. Most failures of PLDs are caused by improperly calibrated test equipment during PLD programming. Over voltaging is the usual problem but it is not the only problem. Under voltaging can stress a specific link and cause it to fail (or set) at a later date.

9. Often PLDs are designed by hand without the aid of schematics and although fuse maps and JEDEC files may be available, a schematic would be valuable to allow the test engineer more insight into internal workings of a circuit.

10. Using "logic reduction" techniques such as Karnaugh maps to implement device designs means having to test fewer internal logic devices and this generates fewer test vectors.

11. Use off-board reset control. Memory power-up reset is better than nothing, but off board reset is preferred since power can remain on during reset rather then powering down and powering up to obtain the required reset condition.

12. Use Electronically Erasable (EE) CMOS PLDs (and flash PLDs) since they can be more easily tested due to not requiring 30 minute erase time between each application of test patterns.

13. The PLD/memories may support pre-loading, but if the tester cannot provide the higher voltage needed, these features will be of little economic value (i.e., separate power supplies will be needed for pre-loading).

14. Avoid unaccessible sequentially deep PLD designs because they are much more difficult to test, require many more test vectors and may make it impossible to test a device fully.

15. Fault tolerant or redundant PLD circuitry may not have to be tested if its failure cannot affect the main circuitry. Thus, without this information many more test vectors have to be developed than necessary.

16. PLD emulators provide a powerful debugging tool and greatly improve testability especially if other forms of testability have not been designed into the circuit.

17. PLD logic descriptions are necessary for the generation of test vectors. Fuse maps in the form of JEDEC files for the individual PLDs can be used to generate test vectors. Joint Electronic Devices Engineering Council (JEDEC) is part of the Electronics Industries Association (EIA). JEDEC files allow the test engineer to understand the internal device's programmed structure for easier test vector generation.

18. Often test equipment software can not convert the files available from the JEDEC format to test vectors. In that case, manual test vector generation is required. Care should be taken to see that the PLDs chosen and the available test equipment are compatible.

10.3 Generic Memory Testability Techniques and Guidelines.

1. Provide access to all memory enable lines and bring the enables out to an edge connector.

2. Design in a method to tri-state individual memory ICs and bring their control lines out to an edge connector.

3. Provide access to all Row Address Strobe (RAS) and Column Address Strobe (CAS) lines.

4. Design the memory so access is available to all memory locations including all "spare" locations in case reprogramming is necessary especially during test.

5. Individual memory ICs should include a checksum value stored in one location in each of the ICs. In this way individual ICs can be checked using the simplest of all memory checks.

6. Provide control to all memory address generators and device enables/disables. Without this control it is impossible to send test patterns to the individual memories to be tested.

7. Design in the ability to go to so called "illegal" memory states so that an entire memory can be tested and not just the sections of the memory that are used for a particular program. Also this allows a test program to reside in this "illegal" memory space.

8. Provide a known output for every ROM input control word, even unused ones. In this way no indeterminate error states can exist.

9. Lay out PLDs so as to minimize shorting possibilities between adjacent lines and thus avoid bridging faults.

10. Design memory PLD in such a way that it is initializable and that unused input pins can be used to externally initialize the device, with as few vectors as possible.

11. Make sure that a PLA power-up state is available. Depending on the manufacturer, PLAs can power-up to all ONEs or all ZEROs.

12. Without an Automatic Test Vector Generator (ATVG), test vectors must be created manually. This can take several months as opposed to several hours or less with ATVG.

13. Complex memory elements are created by one or more interactive feedback loops. This can cause race conditioning during test, even if the final circuit does not race. Generally, these races occur due to a poor understanding of circuit by the ATVG or by the test engineer developing the test. Close cooperation is needed between design and test engineering. First, to avoid feedback loops and second to deal with them if they exist.

15. Use scan in memory devices wherever possible (see section 11). Scan in memory devices allow users to observe input registers and force the state of output registers. Interconnectivity, addresses and data input bus faults can also be tested.

16. Programmable Silicon Circuit Boards (PSCBs) are CCAs which can make resident IC connections programmed by computer. This type of CCA can greatly enhance testability by providing access to internal CCA devices during functional test and repair activity.

10.4 Software Techniques Used for Memory Testability.

1. Memory tests are executed to validate that all memory locations are functional. These tests are normally supplied by the memory device manufacturer. If they are not supplied, they must be generated by the user. Some representative memory test patterns and what each test verifies is listed below:

   a. Zeros. Writing zeros sequentially at each address in memory, the test system then reads the address sequentially.

      This simple N-type test quickly examine either cell opens or cell shorts and the ability to store zeros; however, its main use involves verifying the operation of the hardware interface.

   b. Ones. The system writes ones sequentially at each address in memory, then reads the address sequentially.

      Except for checking the ability to store ones instead of zeros, the ones pattern serves the same purpose as the zeroes pattern.

   c. March. After writing a background of zeroes to memory, the system reads the data at the first address and writes a ONE to this address. The same two-step read-write procedure continues at each sequential cell until the system reaches the end of memory. Each cell is then tested and changed back to ZERO in reverse order until the system returns to the first address. Finally, the test is repeated using compliment data (i.e., writing a background of ones to memory).

      The March pattern is also an N-type pattern. It can find failed cell opens and cell shorts, as well as address uniqueness faults and some cell interaction faults.

   d. Galpat. Into a background of zeroes, the first cell (test cell) is complemented to a ONE and then read alternately with every other cell in memory. This sequence continues as every memory cell becomes the test cell. the system then executes the same sequence using complement data with an execution time proportional to the square of the cell count (N^2 type).

      Galpat looks for cell opens, cell shorts, address uniqueness, sense amplifier interactions, and access time problems (especially those faults related to the address decoder delays).

e. Column Disturb. Into a column of zeroes, the system writes complemented data continually (for a specified time) to the first cell and last cell in one column, then reads data in all other cells, in that column. Then the system restores zeros in the first and last cells and disturbs the second and second-to-last cells, after which the data in the first and last cells are read. This sequence continues for each column in memory. The system then repeats the entire sequence using the complemented data.

Designed to find disturb sensitivities and refresh sensitivity in dynamic RAMs. The pattern's execution time depends on the number of disturb cycles executed.

f. Block Ping-Pong. The address sequencing remains identical to that of Galpat, but the background data consists of alternating blocks of ones and zeroes. The block lengths can be determined by the user. While the Block Ping-Pong pattern has similar execution time and fault-finding capabilities to Galpat, it can also locate some data sensitivity problems that remain undetected by Galpat.

g. Surround Disturb. In a background of zeroes, the system complements the first cell (test cell) and repetitively reads the eight physically adjacent cells (up to 255 times). After reading and restoring the test cell to ZERO, the system continues this procedure until each memory cell has been the test cell. the sequence is then repeated using complemented data.

Surround disturb finds possible adjacent cell disturb malfunctions. Execution time varies with the number of disturb cycles executed at each test cell.

h. Write Recovery. The system writes the second cell to a ONE and reads the first cell (test cell) to a background of zeroes, the second cell is then restored to ZERO and the first cell is read again. The same read/write sequence repeats between the third and the test cell, the fourth and the test cell, and continues to the last and the last test cell. The entire sequence is repeated until every cell has acted as a test cell. Finally, the system repeats the pattern using complemented data.

An N^2 test, the Write Recovery pattern primarily locates write recovery-type faults, although it can also find faults listed under Galpat.

i. Walking Pattern. Into a background of zeroes, the system complements the next cell and reads all other cells sequentially. After reading and restoring the first cell to ZERO, the system complements the first cell and reads all other cells sequentially. This procedure continues for all memory cells. The pattern is then repeated using complemented data.

   The N^2-type walking pattern examines memory devices for cell opens and shorts and address uniqueness.

j. Sliding Bit. Not in itself a pattern, sliding bit merely generates a shifting data pattern and repeatedly calls a test such as March or Galpat to check data bit uniqueness in multi-data chips or boards.

k. Checkerboard Read/Write. This program writes a checkerboard (alternating zeroes and ones into memory; a control program or delay subroutine then executes a delay before the system reads the checkerboard pattern. Not-checkerboard Read/Write patterns can provide complemented data patterns.

   Usually employed in conjunction with a long delay (typically measured in seconds) between the write and read parts of a test, the N-type checkerboard patterns (with delay) evaluate static and data retention in static RAMs.

Other memory test patterns include: Address Test, Moving Inversion (MOIV), Row Disturb, Row Galpat, Column Galpat, Sliding Diagonal, Buffer Write Surround Disturb,and Buffer Ping-Pong.

Before the above tests are chosen it is wise to check if the available tester can support them. Alternating complementary test patterns, such as a checkerboard pattern, March, Galpat, etc., may be required to completely test a device, but the available tester may not have the capability to generate them and interpret the results. Also, the device may be designed in such a manner that access is not available to all address lines (i.e. unused or spare lines).

SECTION 11. STRUCTURED DESIGN-FOR-TEST TECHNIQUES

11.0 OVERVIEW.

This section describes structured design-for-test (DFT) techniques which employ scan methods. Scan designs are usually implemented only to improve the testability of a custom device during device testing. However, some scan techniques, such as boundary scan, greatly improve the testability of every level of configuration containing scan devices.

Since scan circuitry is designed into a device, a decision to use a scan technique must be made early in the design phase.

It is predicted that the use of IEEE STD-1149.1 boundary scan will become commonplace in the near future. Consequently, most of this section describes the boundary scan technique and boundary scan recommendations.

11.1 Structured LSI/VLSI.

Today, with the utilization of LSI and VLSI technology, it has become apparent that even more care will have to be taken in the design stage to ensure testability and producibility of custom devices and digital networks. This has led to rigorous and highly structured design practices.

Most structured design practices are built on the following concepts:

1. Provide additional access to internal nodes of a circuit without a separate external connection for each node accessed. (Accessibility)

2. Direct control of all internal latch states. (Controllability)

3. Direct observation of all internal latch states. (Observability)

Besides improved accessibility, sequential circuit test pattern generation is not required. If the latches can be tested directly only combinatorial test pattern generation is needed. This reduces the test generation and fault simulation costs greatly, especially if an Automatic Test Pattern Generator (ATPG) can be used.

A common feature of scan methods is serialization of test patterns , as many internal nodes need to be accessed with a minimal increase in external I/O. As there are more internal nodes than external I/O, the test patterns need to be transmitted and received serially (scanned) in and out of the circuit.

11.1.1 Level Sensitive Scan Design (LSSD). LSSD is a popular IBM discipline for structural DFT. Scan refers to the ability to shift into or out of any state of the network. Level-sensitive refers to constraints on circuit excitation, logic depth, and the handling of clocked circuitry. A key element in the design is the shift register latch (SRL).

One implementation of an LSSD SRL is shown in figure 11-1. In this example figure (a) shows an SRL block diagram and figure (b) shows the actual SRL logic. Such a circuit is immune to most anomalies in the AC characteristics of the clock, requiring only that it remain high (sample) at least long enough to stabilize the feedback loop before being returned to the low (hold) state. The lines D and C form the normal mode memory function while lines I, A, B, and L2 comprise additional circuitry for the shift register function.

Figure 11-2 shows a generalized sequential circuit model modified to use a shift register. This technique allows both controllability and observability, allowing the testing to be augmented by controlling inputs and internal states, and easily examining internal state behavior. An apparent disadvantage is the serialization of the test, potentially costing more time for actually running the test.

The shift registers are threaded by connecting outputs (L2) to inputs (I) and operated by clocking lines A and B in two-phase fashion (see figure 11-1). Figure 11-3 shows four modules threaded for shift register action. In figure 11-3 each module could be an SRL or, one level up, a board containing threaded ICs, etc. Each level of packaging requires the same four additional lines to implement the shift register scan feature.

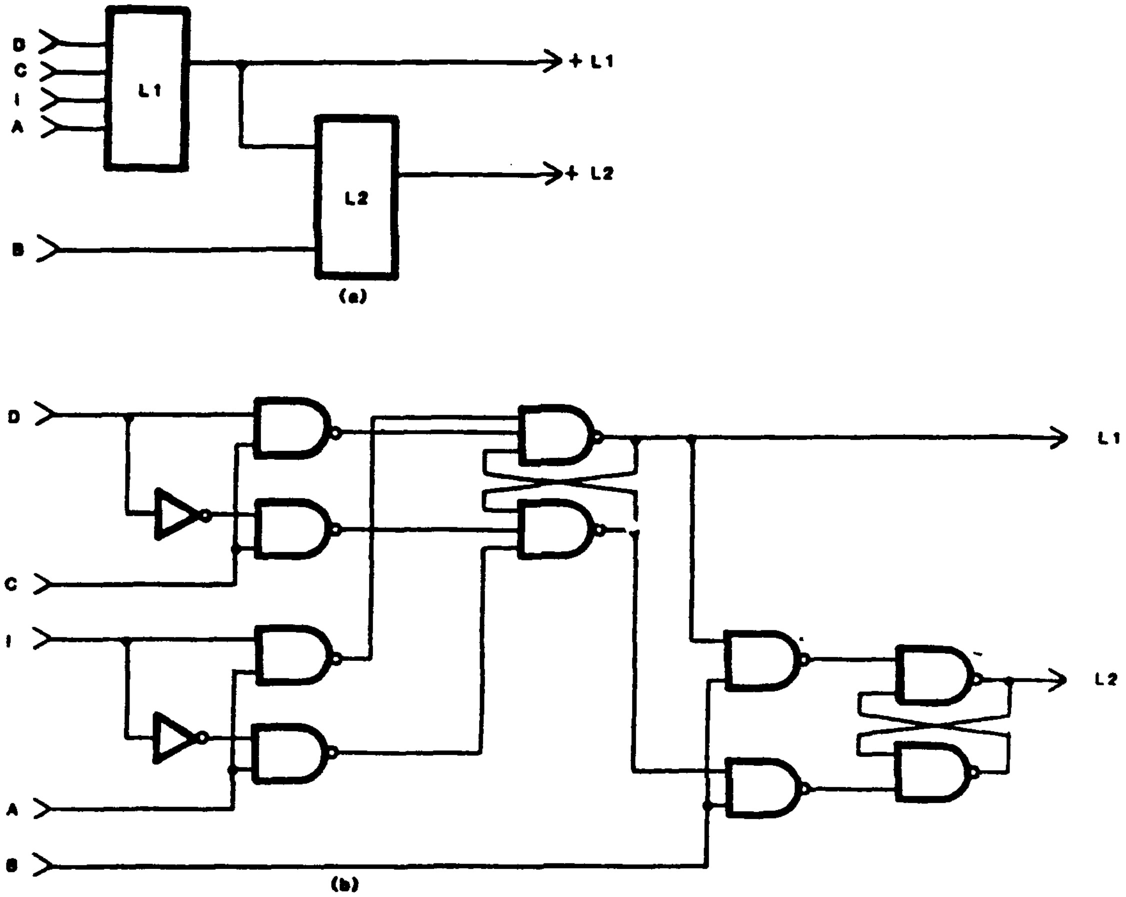


Figure 11-1. Level Sensitive Scan Design Shift Register Latch (SRL)

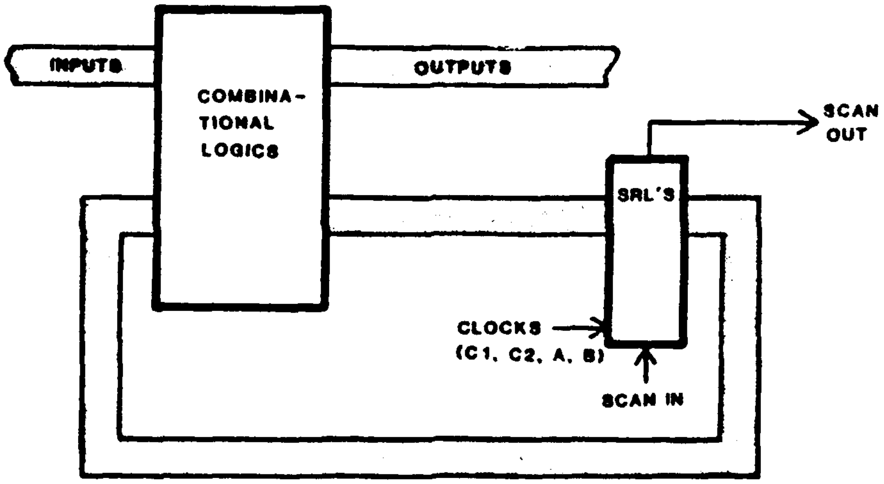


Figure 11-2. Placement of SRLs in Sequential circuit

Figure 11-4 depicts a general structure for an LSSD subsystem with a two-phase system clock. It is not practical to implement RAM with SRL memory, so additional procedures are required to handle embedded RAM circuitry.

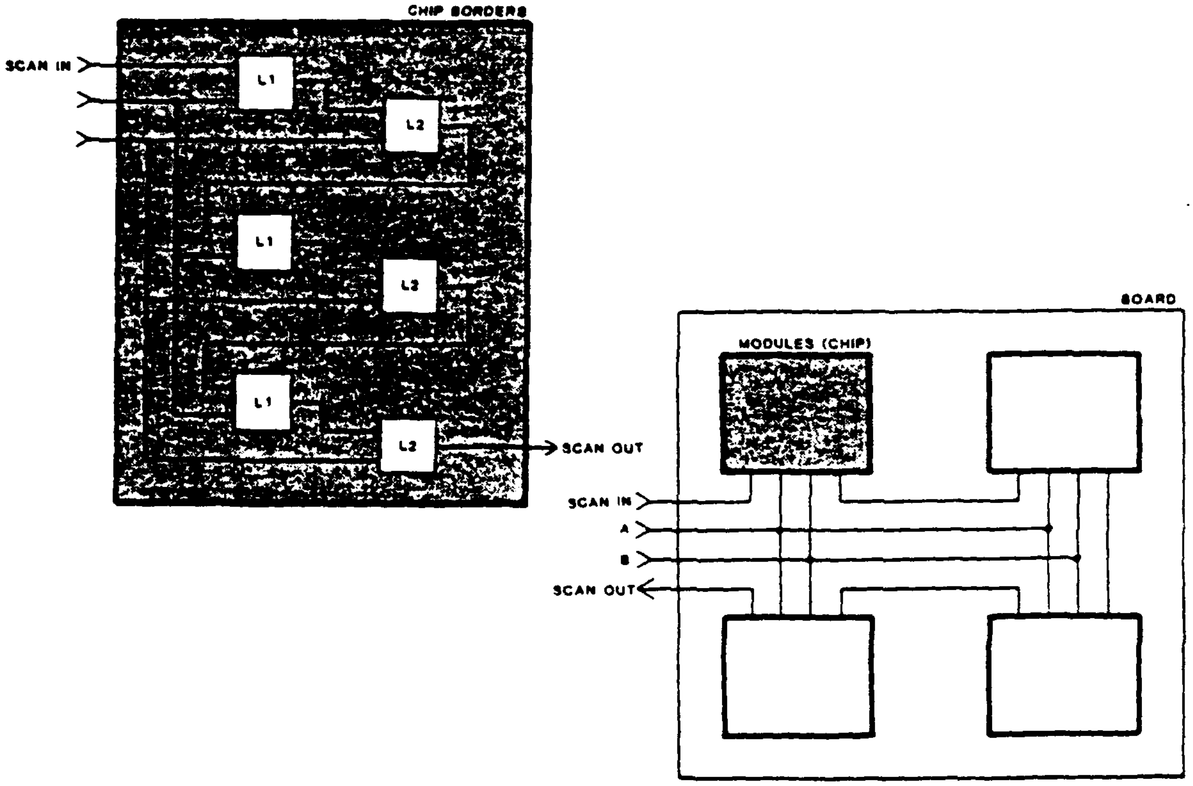


Figure 11-3. Shift Register Chain

Given that an LSSD structure is achieved, what are the rewards? The network can now be thought of as purely combinational, where tests are applied via primary inputs and shift register outputs. The testing of combinational circuits is a well understood and (barely) tractable problem.

In considering the cost performance impacts, there are a number of negative impacts associated with the LSSD design philosophy. The latches in the shift register are, logically, two or three times as complex as simple latches. Up to four additional primary inputs/outputs are required at each package level for control of the shift registers. External asynchronous input signals must not change more than once every clock cycle. Finally, all timing within the subsystem is controlled by externally generated clock signals.

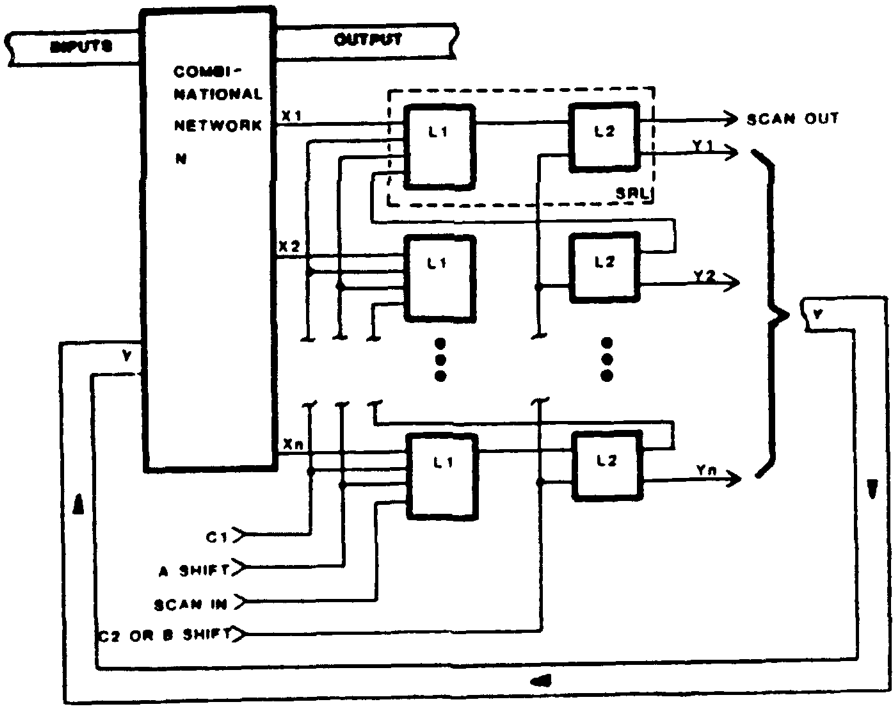


Figure 11-4. LSSD Subsystem with a Two-Phase System Clock

The LSSD structured design approach for design for testability eliminates or alleviates some of the problems in designing, manufacturing, and maintaining LSI systems at a reasonable cost.

11.1.2 Scan Path. The scan path technique has the same objectives as the LSSD approach described above. The memory elements that are used are shown in figure 11-5. The memory element is called a raceless D-type flip-flop with scan path.

In system operation, clock 2 is at a logic value of 1 for the entire period. In essence, this blocks the test or scan input from affecting the values in the first latch. This D-type flip-flop really contains two latches. Also, by having clock 2 at a logic value of 1, the values in latch 2 are not disturbed.

Clock 1 is the sole clock in system operation for the D-type flip-flop. When clock 1 is at a value of 0, the system data input can be loaded into latch 1. As long as clock 1 is 0 for sufficient time to latch up the data, it can then turn off. It will make latch 2 sensitive to the data output of latch 1. As long as clock 1 is equal to a 1 so that data can be latched up into latch 2, reliable operation will occur.

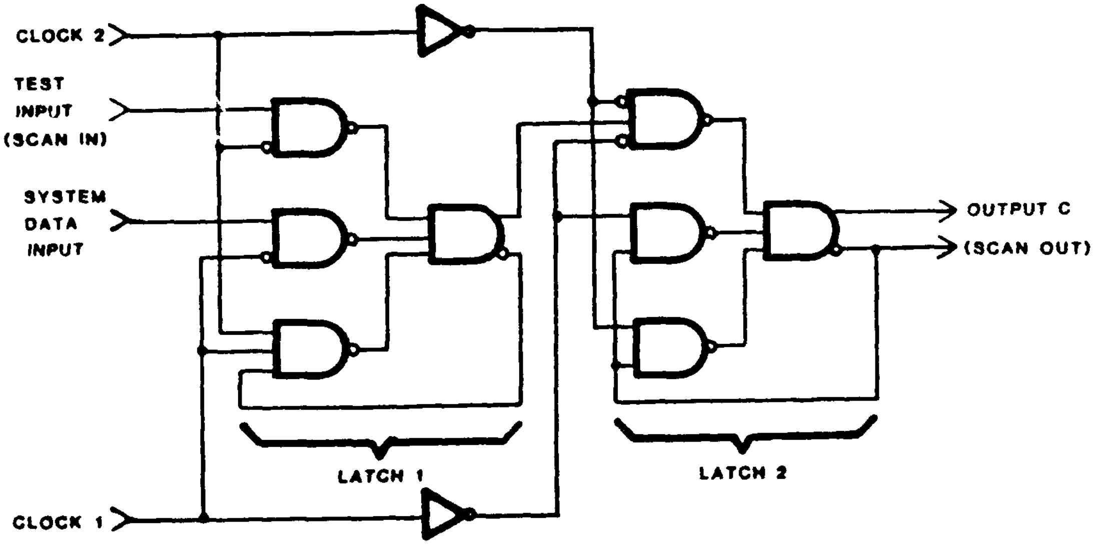


Figure 11-5. Scan Latch Used in Scan Path

In terms of the scanning function, the D-type flip-flop with scan path has its own scan input called test input. This is clocked into the L1 latch by clock 2 when clock 2 is a 0, and the results of latch 1 are clocked into latch 2 when clock 2 is a 1. Again, this applies to master/slave operation of latch 1 and latch 2 with its associated race. With proper atte¬tion to delays, this race will not be a problem.

Another feature of the scan path approach is the configuration used at the logic card level. All modules on the logic card are connected into a serial scan path, such that for each card there is one scan path. In addition, there are gates for selecting a particular card in a subsystem. In figure 11-6, when X and Y are both equal to 1, clock 2 will be allowed to shift data through the scan path. Any other time, clock 2 will be blocked and so will its output. The reason for blocking the output is that a number of card outputs can then be put together; thus, the blocking function will put their outputs to noncontrolling values so that a particular card can have unique control of the unique test output for that system.

Other than the lack of the level sensitive attribute to the scan path approach, the technique is very similar to the LSSD approach. The scan path approach was the first practical implementation of shift registers for testing, which was incorporated in a total system.

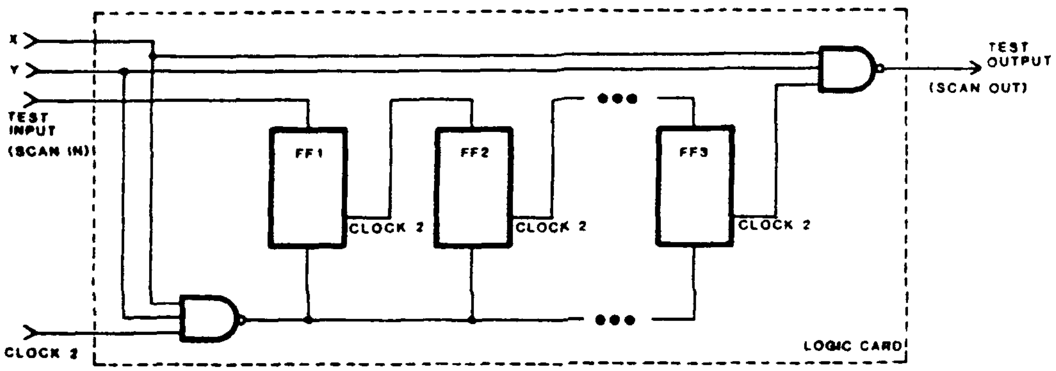


Figure 11-6. Connecting Scan Paths in a Serial Chain

11.1.3 Scan/Set Logic. A technique similar to scan path and LSSD is the scan/set technique. The basic concept of this technique is to have shift registers (as in scan path or in LSSD) but these shift registers are not in the data path. That is, they are not in the system data path, they are independent of all the system latches. Figure 11-7 is an example of the scan/set logic, referred to as bit- serial logic.

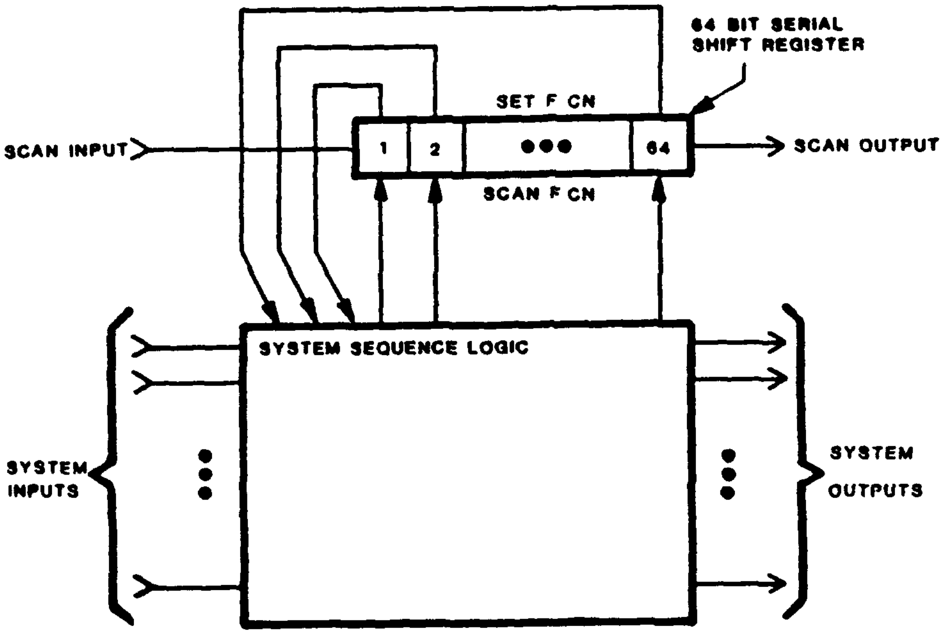


Figure 11-7. Scan/Set Logic

The basic concept is that the sequential network can be sampled at up to 64 points. These points can be loaded into the 64-bit shift register with a single clock. Once the 64 bits are loaded, a shifting process will occur, and the data will be scanned out through the scan-out pin. In the case of the set function, the 64 bits can be funnelled into the system logic, and the appropriate clocking structure required to load data into the system latches is required in this system logic. Furthermore, the set function also could be used to control different paths to ease the testing function.

In general, this serial scan/set logic would be integrated onto the same chip that contains sequential system logic. However, some applications have been put forth where the bit serial scan/set logic was off-chip, and the bit-serial scan/set logic only sampled outputs or drove inputs to facilitate in-circuit testing (section 15).

It is not required that the set function set all system latches or that the scan function scan all system latches. This design flexibility would have a reflection in the software support required to implement such a technique.

Another advantage of this technique is that the scan function can occur during system operation. That is, the sampling pulse to the 64-bit serial shift register can occur while system clocks are being applied to the system sequential logic, so that a snapshot of the sequential machine can be obtained and off-loaded without any degradation in system performance.

11.1.4 Random Access Scan. Another technique similar to the scan path technique and LSSD is the random access scan technique. This technique has the same objective as scan path and LSSD - that is, to have complete controllability and observability of all internal latches. The test generation function can be reduced to that of combinational test generation and combinational fault simulation as well.

Random Access Scan differs from the other two techniques in that shift registers are not employed. An an addressing scheme is employed which allows each latch to be uniquely selected, so that it can be either controlled or observed.

Figures 11-8 and 11-9 show the two basic latch configurations that are required for the random access scan approach. Figure 11-8 is a single latch, which has added to it an extra data port - a scan data in (SDI) port. This data is clocked into the latch by the SCK clock. The SCK clock can affect this latch only if both the X and Y address are 1. When the Z and Y addresses are 1, the scan data out (SDO) port can be observed.

System data labeled Data in figures 11-8 and 11-9 are loaded into this latch by the system clock labeled CK.

The set/reset-type addressable latch in figure 11-9 does not have a scan clock to load data into the system latch. This latch is first cleared by the CL line, and the CL line is connected to other latches that are also set/reset type addressable latches. This then places the output value Q to a 0 value. For those latches that are required to be set to a 1 for that particular test, a preset is directed at those latches. This preset is directed by addressing each one of those latches and applying the preset pulse labeled PR. The output of the latch, Q, will then go to a 1.

The observability mechanism for scan data out is exactly the same as for the latch shown in figure 11-8.

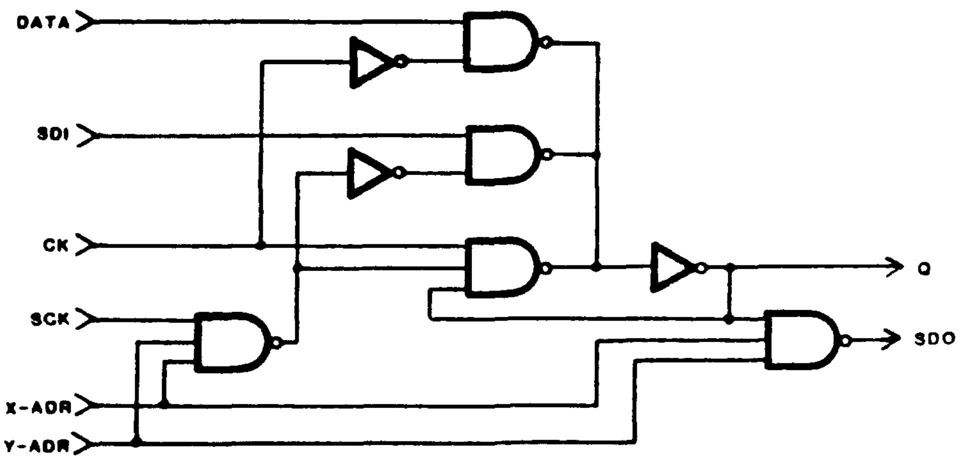


Figure 11-8. Basic Random Access Scan Latch

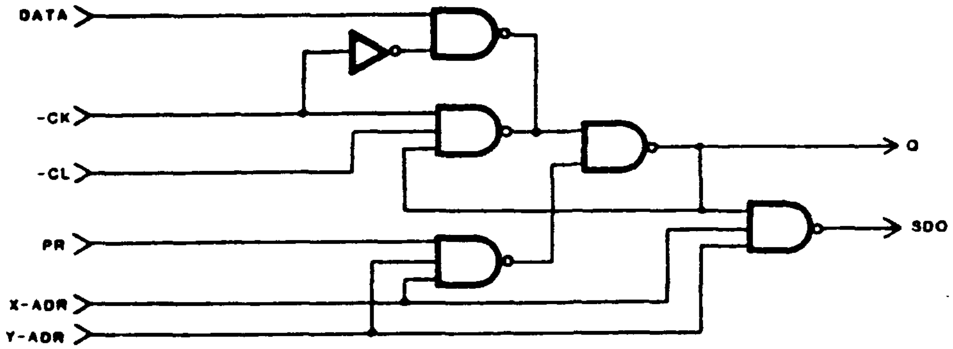


FIGURE 4-17

Figure 11-9. Set/Reset Random Access Scan Latch

Figure 11-10 gives an overall view of the system configuration of the random access scan approach. Basically, there is a Y address, an X address, a decoder, the addressable storage elements, which are the memory elements or latches, and the sequential machine, system clocks, and CLEAR function. There is also a scan data in (SDI), which is the input for a given latch, scan data out (SDO), which is the output data for that given latch, and a scan clock. There is also one logic gate which is necessary to create the preset function.

The random access scan technique allows the observability and controllability of all system latches. In addition, any point in the combinational network can be observed with the addition of one gate per observation point, as well as one address in the address gate per observation point.

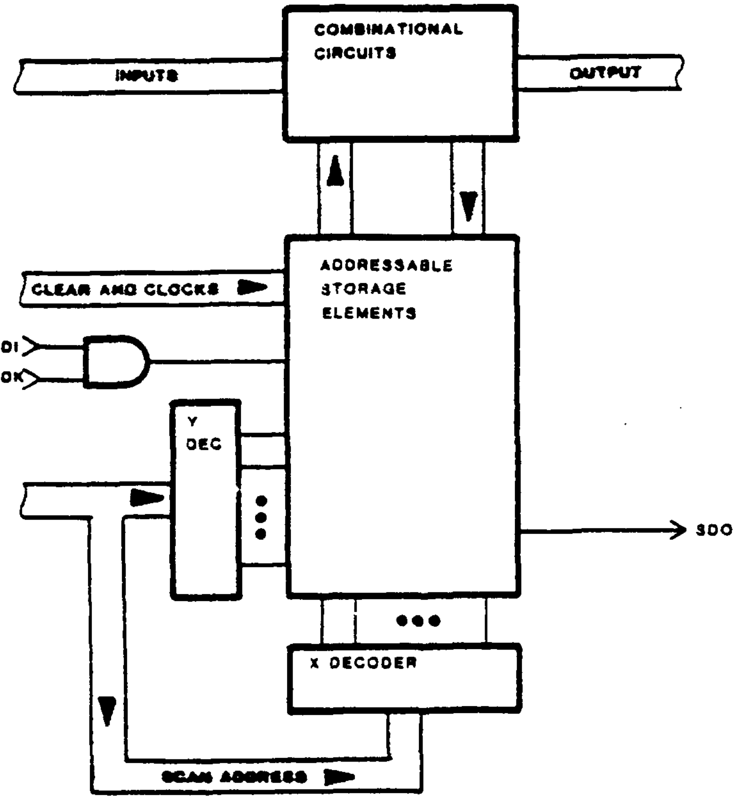


Figure 11-10. Random Access Scan in a System

11.1.5 Built-in Logic Block Observation (BILBO). This technique takes the scan path and LSSD concept and integrates it with the signature analysis concept (see section 6.2.2). The end result is a technique called BILBO. BILBO is a form of Built-in Test (BIT) and is described in section 6.

11.2 Boundary Scan - 1149.1.

11.2.1 Introduction. Many complex digital circuit designs are extremely difficult to test functionally. In some cases in-circuit test (see section 15) is an easy solution to a complex test problem. However, due to the use of surface mount technology (SMT) and Application Specific Integrated Circuits (ASICs) many designs have limited node access and cannot be in-circuit tested. Conformal coating and test requirements may also restrict the use of in-circuit test.

One way to make a complex digital circuit design more testable is to use a structured design-for-test (DFT) approach - circuitry designed specifically for test is implemented in digital devices used in the circuit. The most common structured DFT approach is scan. There are many types of scan designs, most of which use shift register latches (SRL) to enhance the observability and controllability of a design/device.

Boundary Scan is a scan technique used specifically to enhance the testability of a board and every higher level of configuration. When a device is designed with boundary scan, it is possible to control and observe all primary input and output pins of the device using only four device pins. If all devices on a board are implemented with boundary scan, every device can be tested using only four serial connector pins plus power and ground signals. This section (11.2) discusses how boundary scan can be implemented and the resulting testability when boundary scan is used.

First, boundary scan test circuitry will be described, then a device with boundary scan, a board with boundary scan and, finally, boundary scan enhancements.

11.2.2 History. For the past 20 years there have been a multitude of scan practices. In 1985 a group of companies (mostly European) called the Joint Test Action Group (JTAG) suggested that Boundary Scan be considered as an IEEE standard. In 1990 the JTAG Boundary Scan suggestion was implemented as IEEE Standard 1149.1.

The remainder of this section will describe boundary scan based on the 1149.1 standard. The concept of boundary scan can be implemented without following the standard. However, this standard should be followed as closely as possible.

11.2.3 Testability Problem. As an example of a design with testability problems, consider figure 11-11. In this design two SMT ASICs are in series. To test device B, signals need to be propagated through device A and the runs between the pins of device A and B. This causes two problems:

1. Development of tests for device B is sophisticated - input signals of device B must first be propagated through device A.

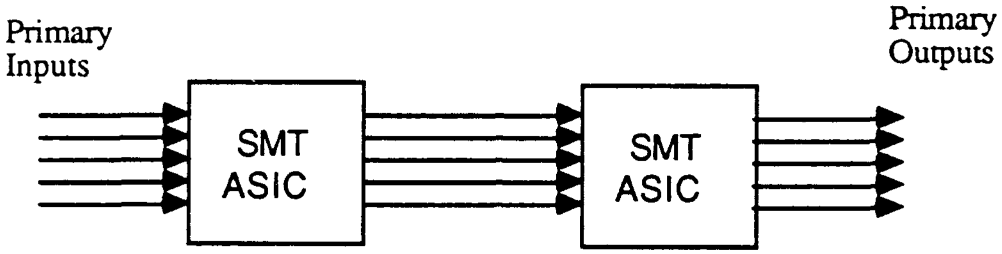


Figure 11-11. Circuit with Testability Problems

2. Fault detection - if an incorrect signal is observed at an output of device B, the failure could have been caused by device A, device B, or any run between the pins of device A.

An ideal case of testability would be to have direct controllability and observability at every pin of each device.

A typical test solution would be an in-circuit tester using a bed-of-nails fixture for node access. This can be both difficult and costly to produce due to the following factors:

1. Closely spaced SMT device pins (<50 mil)

2. Expensive and unreliable fixturing for dual-sided SMT boards.

3. Lengthy ASIC test vectors overdriving upstream devices (can cause damage to overdriven upstream devices).

Functional board test via the board I/O pins is an undesirable alternative due to the lengthy and expensive test generation process, especially if the devices used are poorly documented or have inherent testability problems. Unfortunately, this is too often the case with both commercial and custom LSI devices.

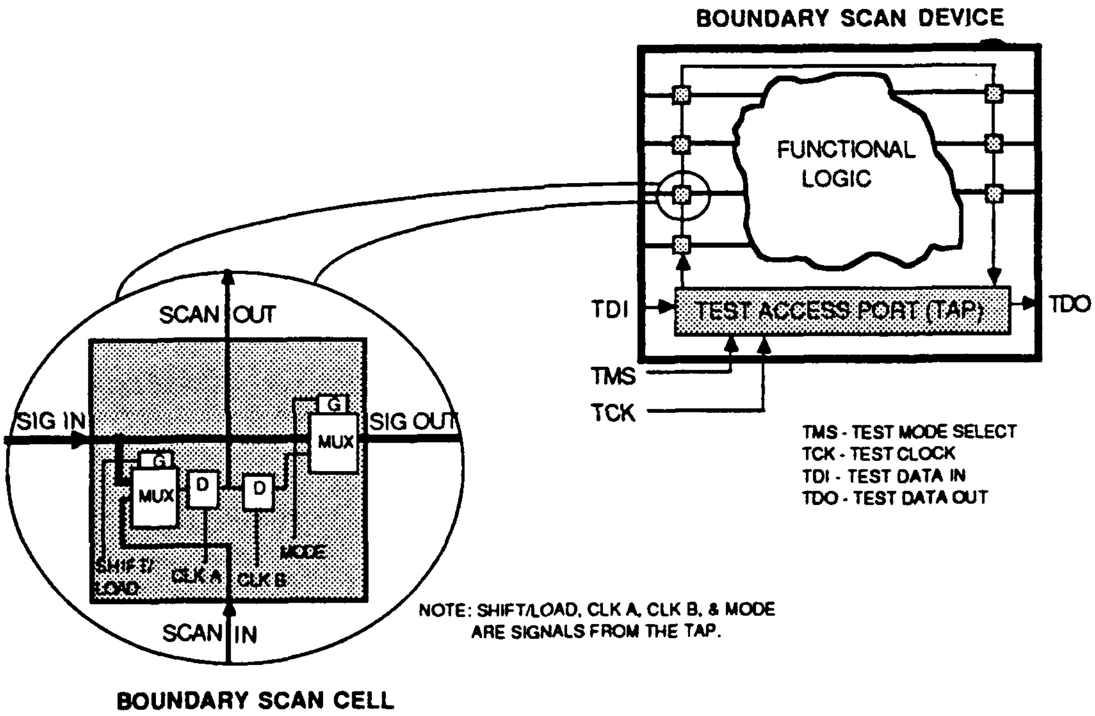
By consciously designing or selecting devices with boundary scan, the designer enables boards to be tested using the equivalent of an in-circuit test but without physical probing and without overdriving any device outputs.

Using only four board test nodes, boundary scan allows detection of the same spectrum of manufacturing defects as in-circuit test, such as shorts/opens, wrong components, or missing components. It also allows circuit activity to be observed during normal functional operation. Similar to in-circuit testing, boundary scan does not verify functional "at speed" performance.

11.2.4 Boundary Scan Implementation.

11.2.4.1 Device Level Implementation.

11.2.4.1.1 Boundary Scan Cells. Boundary scan can be designed directly into a device using shift register latches (SRLs) and control circuitry. For the remainder of this section a boundary scan SRL will be referred to as a cell. An example of a device designed with boundary scan is shown in figure 11-12.



TMS - TEST MODE SELECT
TCK - TEST CLOCK
TDI - TEST DATA IN
TDO - TEST DATA OUT

NOTE: SHIFT/LOAD, CLK A, CLK B, & MODE ARE SIGNALS FROM THE TAP.

Figure 11-12. Example of a Boundary Scan Cell

The cell shown is only one example of a cell design. Referring to figure 11-12, the area marked as "functional logic" in the ICs is the IC circuitry used for functional operation.

From the exploded view of a boundary scan cell, it is easy to analyze the possible functions of the cell. Inside each device, boundary scan cells are interposed between the IC functional logic and each physical device pin. The cell can operate as follows:

1. Pass the signal from "Signal In" directly to "Signal Out" (normal functional operation).

2. Pass the signal from "Signal In" to "Signal Out" and load a D flip-flop with "Signal In" (sample).

3. Pass the signal from "Signal In" to "Signal Out", load a D flip-flop with "Scan In", and send the contents of the first D flip-flop to "Scan Out" (similar to one shift register).

4. Pass the contents of the D flip-flop to "Signal Out".

(Note that the control signals in the boundary scan cell are generated from the Test Access Port (TAP).)

11.2.4.1.2 Boundary Scan Chain. By connecting "Scan Out" of one cell to "Scan In" of another cell a shift register can be formed. In boundary scan devices the boundary scan cells are connected in this manner to form a boundary scan chain. This chain can act as a serial shift register.

In one mode of operation the boundary scan device can shift data into the boundary scan chain, pulse it into the device functional logic, sample the functional logic output, and shift the sampled data out. This is analogous to putting one test pattern into a device and observing its output.

Notice that every device I/O signal can be controlled or observed by the boundary scan cells independently of any exterior connections.

An average of 5 to 20 percent device area is used by boundary scan circuitry when implemented. Also, signals travelling through boundary scan cells are delayed through the multiplexer (MUX). (About 1 ns for input signals and 1.5 ns for outputs.)

11.2.4.1.3 Test Access Port (TAP). The TAP is a feature of the IEEE STD 1149.1. Basically, it is a state machine that can configure any on-chip testability features and provides the control lines to the boundary scan cells. A minimum of four device I/O pins are needed to access the TAP as follows:

TMS = Test Mode Select - Serial control signal which controls the state of the TAP.

TCK = Test Clock

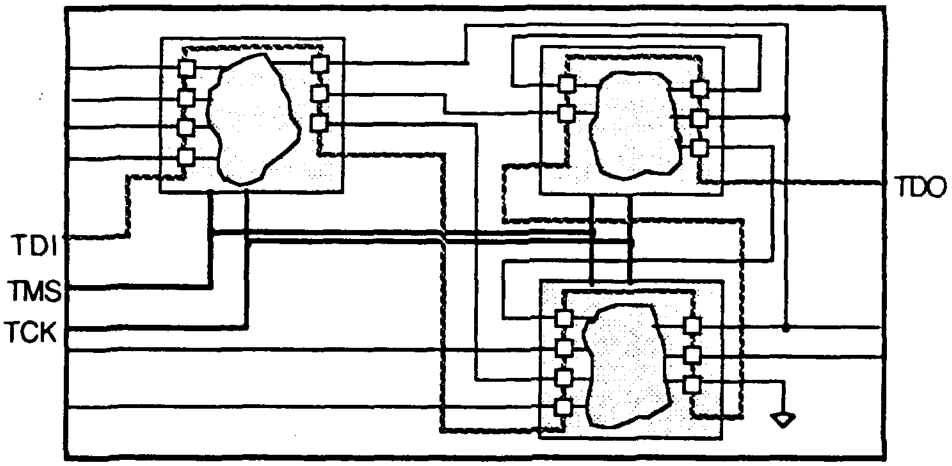
TDI = Test Data In - Serial data signal which can be used to input an instruction to the TAP or input test data to scan cells.

TDO = Test Data Out - Serial signal used to output data from scan cells.

During normal operation the TAP is inactive. During test, TMS is first set to allow the TAP to load a serial instruction from TDI. This instruction will tell the TAP what series of operations to execute. The figures on the following pages show boundary scan devices. Each device has a TAP (all boundary scan devices must have a TAP) but the TAP is not shown in the figures in order to simplify the diagrams.

11.2.4.2 Board Level Implementation. Figure 11-13 shows one implementation of boundary scan devices in a design. In this example, TDO of one device is tied to TDI of another. The cells of all three devices can be connected as one long boundary scan chain for loading and observing data. As shown, there are three required instructions in the IEEE 1149.1 boundary scan standard and two recommended optional instructions.

Note: A design may offer additional instructions for design-specific features.



P1149.1 REQUIRED INSTRUCTIONS:

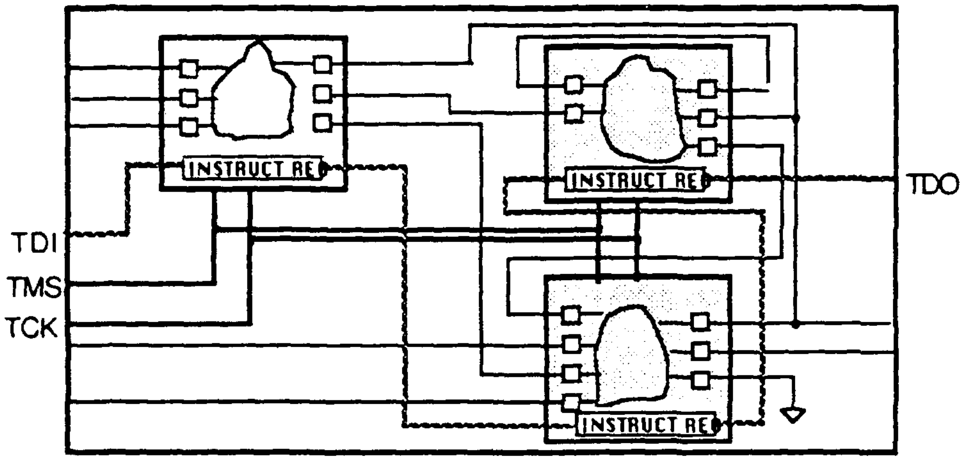
- EXTEST
- BYPASS
- SAMPLE

OPTIONAL INSTRUCTIONS

- RUNBIST
- INTEST

Figure 11-13. Board Level Implementation of Boundary Scan

11.2.4.3 Instructions. To initiate a boundary scan instruction, a signal is sent from TMS to get the TAP to accept an instruction from TDI (instruction registers placed in a shift register mode of each device are placed in the path from TDI to TDO). At this point, the individual latches of the instruction registers of each device should initialize to 00...01 where 00 are the two most significant latches. (It is required that the least two significant bits initialize to 01). Next, a series of instructions are serially shifted into device instruction registers (IR) from TDI until all instructions are shifted into the correct device cells. See figure 11-14. While data is being shifted into instruction registers, the values initially in the instruction registers are shifted out TDO. Since each IR was initialized to ...01, output data shifted out the IRs can be used to confirm the integrity of the Test Access Port (TAP).



P1149.1 REQUIRED INSTRUCTIONS:
- EXTEST
- BYPASS
- SAMPLE

OPTIONAL INSTRUCTIONS
- RUNBIST - IDCODE
- INTEST - USERCODE

Figure 11-14. Loading a Boundary Scan Instruction

11.2.4.3.1 EXTEST. - (Required instruction) For testing board interconnects. A TDI serial data signal is serially loaded into the boundary scan chain, clocked onto the device output pins, sampled by input cells at input device pins, and serially shifted out TDO to verify the data. This instruction is used to verify there are no short or open PCB traces between boundary scan devices. It also confirms that all the boundary scan device I/O pins are operational. Connector signals are transmitted and received between test equipment at connector pins and boundary scan devices during this test. See figure 11-15.

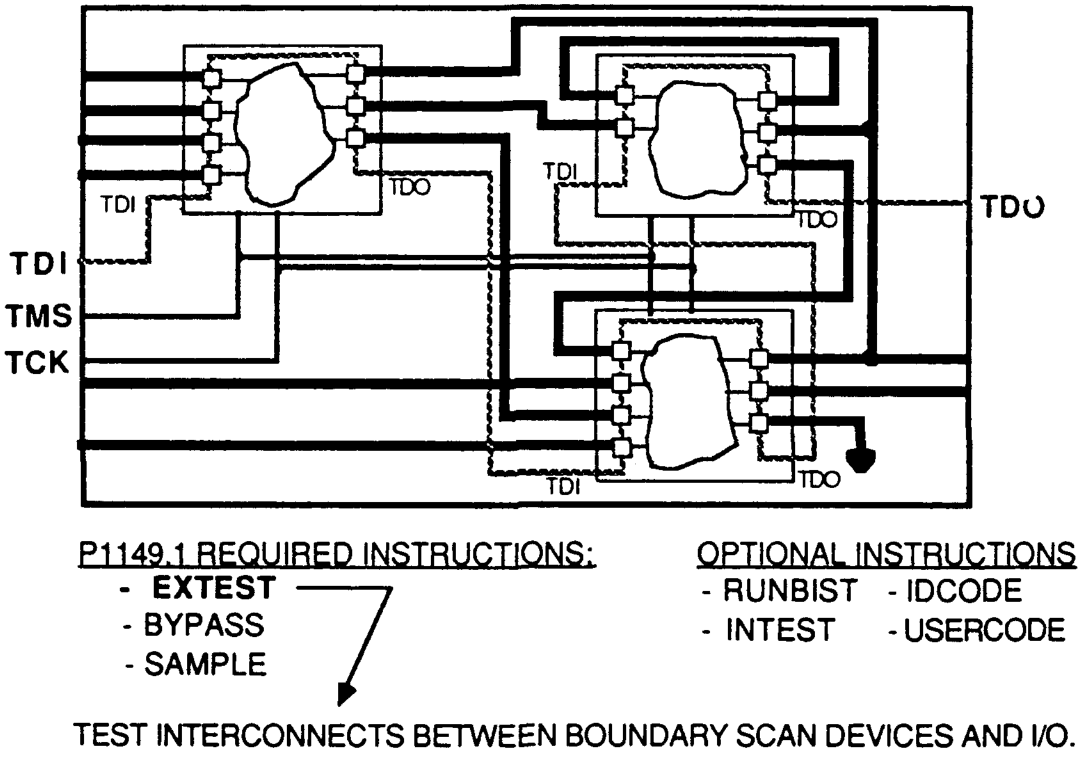
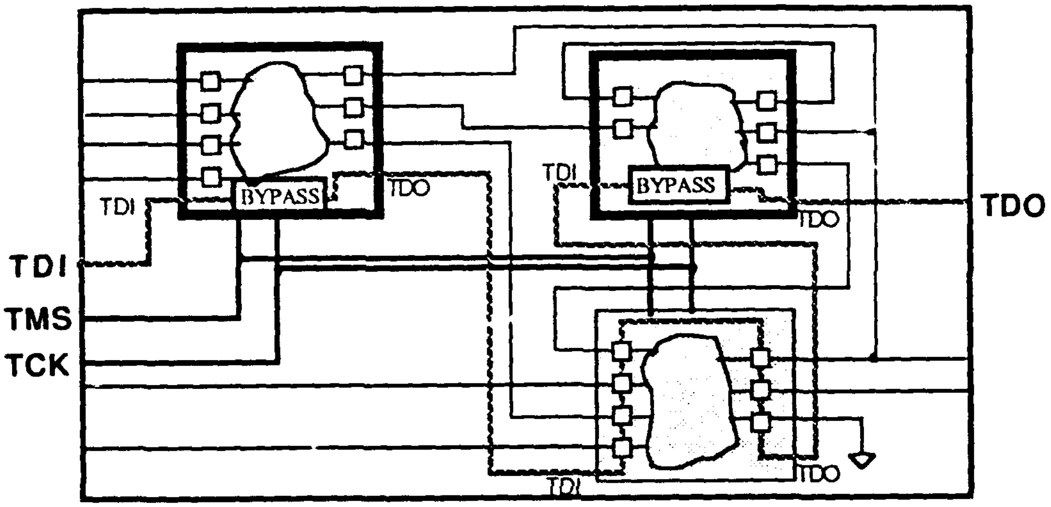


Figure 11-15. EXTEST Instruction

11.2.4.3.2 BYPASS. - (Required instruction) For devices not undergoing the present test. Replaces the boundary scan chains on a device with a one cell bypass shift register. When a device is being tested, this instruction is used to bypass other devices in the scan path that are not being tested. By using this mode, the number of serial test vectors required for boundary scan is reduced enormously. Data being serially loaded to and from a device under test does not have to travel through every scan cells of each device in the scan path. Instructions which are not supported by a device are equivalent to the BYPASS instruction. See figure 11-16.



P1149.1 REQUIRED INSTRUCTIONS:

- EXTEST
- BYPASS
- SAMPLE

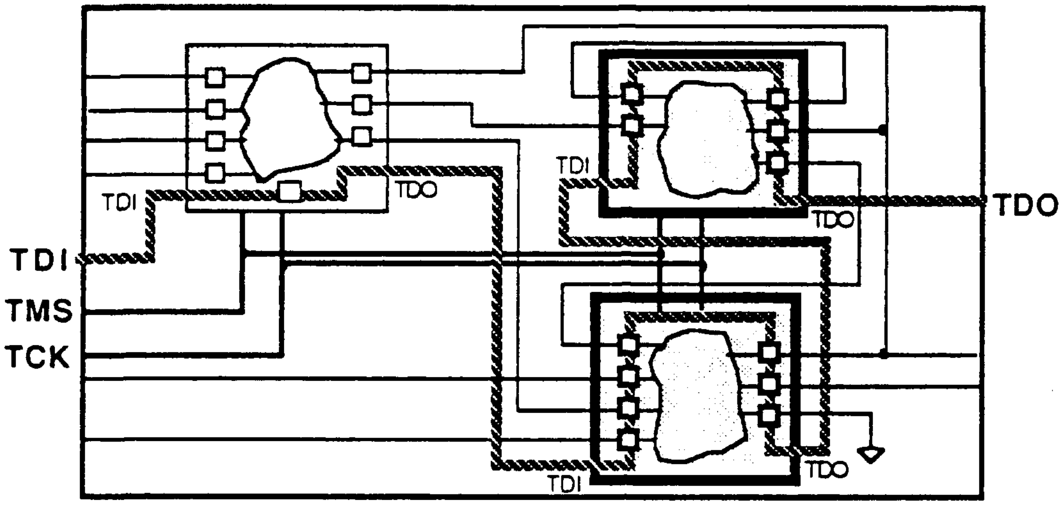
OPTIONAL INSTRUCTIONS

- RUNBIST
- INTEST
- IDCODE
- USERCODE

BOUNDARY SCAN PATH REPLACED BY ONE CELL.
DOES NOT AFFECT DEVICE FUNCTIONAL OPERATION.

Figure 11-16. BYPASS Instruction

11.2.4.3.3 SAMPLE. - (Required instruction). Sample data boundary scan cells. Signals at a devices functional I/O are sampled and stored in the boundary scan cells, then serially shifted out TDO for observation. This enables a snapshot of the board function and can be used to debug the design or aid fault diagnosis without interfering with the board or system operation. See figure 11-17.



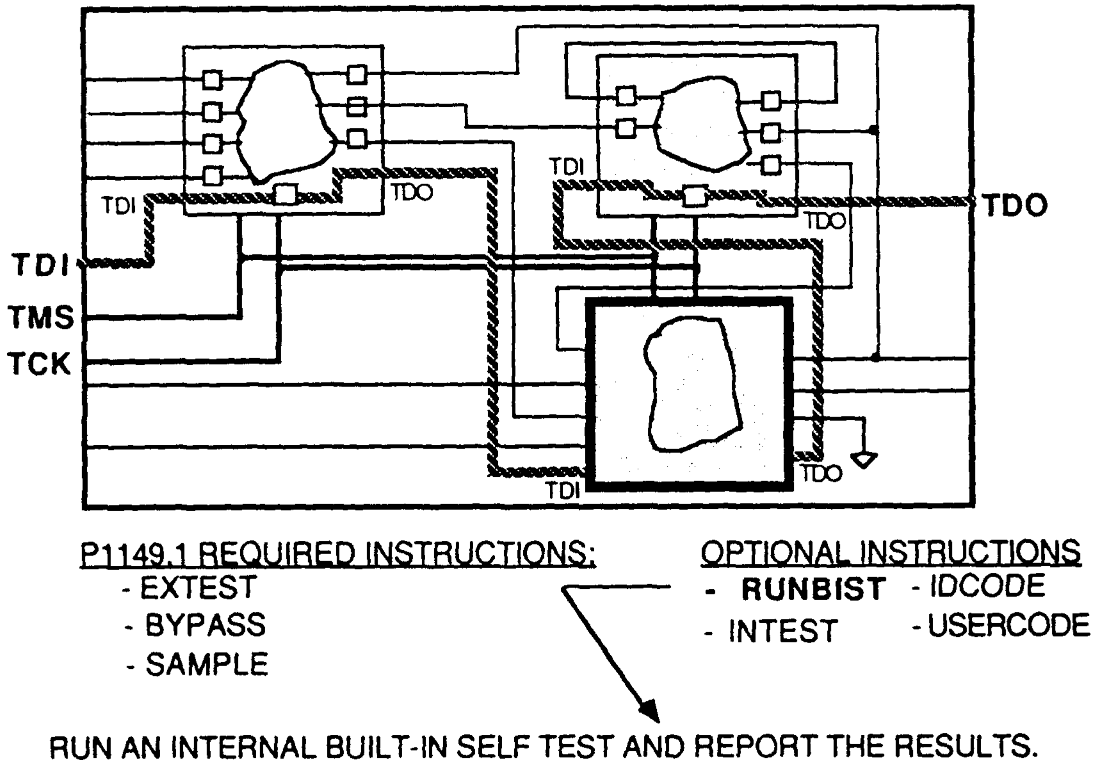
P1149.1 REQUIRED INSTRUCTIONS:
- EXTEST
- BYPASS
- **SAMPLE**

OPTIONAL INSTRUCTIONS
- RUNBIST
- IDCODE
- INTEST
- USERCODE

SAMPLE THE SIGNAL AT DEVICE'S BOUNDARY SCAN CELLS AND SHIFT OUT.
DOES NOT AFFECT DEVICE FUNCTIONAL OPERATION.

Figure 11-17. SAMPLE Instruction

11.2.4.3.4 RUNBIST. - (Optional instruction) Run Built-in Self-Test (BIST). This instruction tells a device to run its own internal BIST. One way to configure RUNBIST is to have the boundary scan cells at the device input and output act as two Linear Feedback Shift Registers (LFSRs). The LFSR using the input boundary scan cells can act as a pseudorandom number generator and the cells at the output can act as a signature analyzer. The input cell LFSR can generate random data. After a certain number of clocks, the output cell LFSR can be sampled and shifted out TDO to verify a proper signature. Section 6 contains a description of signature analysis. See figure 11-18.



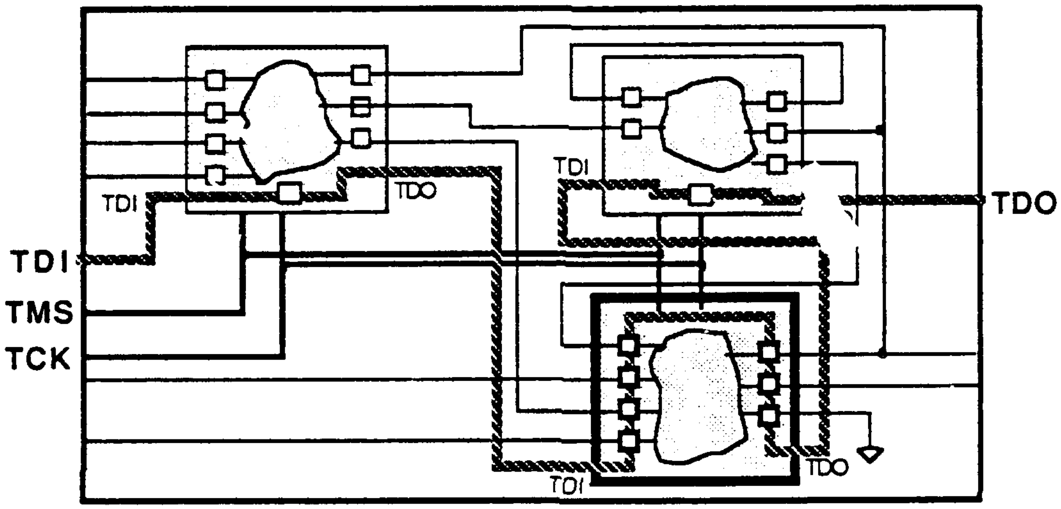
P1149.1 REQUIRED INSTRUCTIONS:
- EXTEST
- BYPASS
- SAMPLE

OPTIONAL INSTRUCTIONS
- **RUNBIST** - IDCODE
- INTEST - USERCODE

RUN AN INTERNAL BUILT-IN SELF TEST AND REPORT THE RESULTS.

Figure 11-18. RUNBIST Instruction

11.2.4.3.5 INTEST. - (Optional instruction) Test device internal logic. Device test data is serially loaded into boundary scan cells via TDI, clocked into device functional logic, sampled at output cells, and serially shifted out TDO for validation. This is repeated for every pattern needed to test a device. The INTEST instruction is targeted at using existing device test vectors provided from the device design or manufacturing process. The advantage of this lies in reduced test generation costs and excellent diagnostics to the failing device. Also note that the device test is independent of its interconnects on the board. See figure 11-19.



P1149.1 REQUIRED INSTRUCTIONS:
- EXTEST
- BYPASS
- SAMPLE

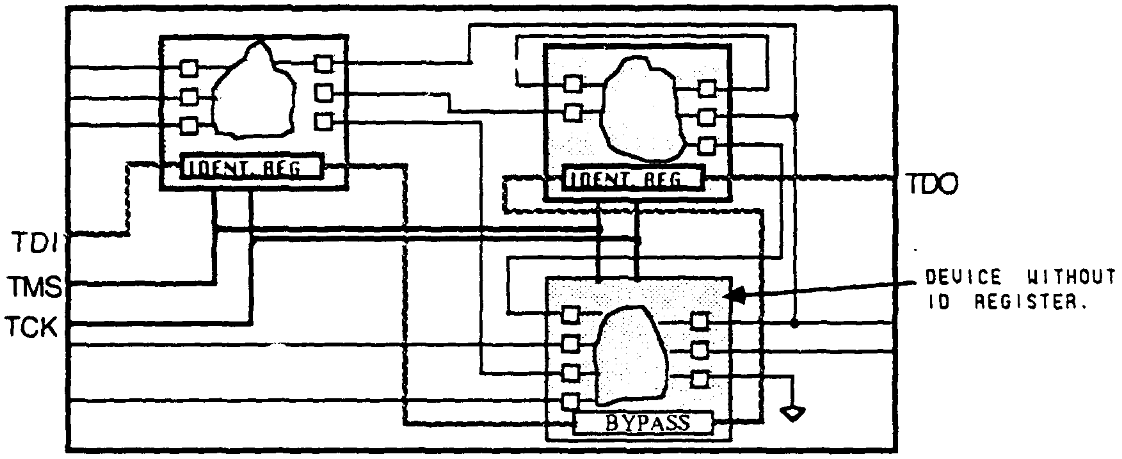
OPTIONAL INSTRUCTIONS
- RUNBIST - IDCODE
- **INTEST** - USERCODE

SHIFT DATA INTO BS CELLS. PULSE INTO DEVICE. SAMPLE OUTPUT.

Figure 11-19. INTEST Instruction

11.2.4.3.6 ID CODE. - Device identification. This instruction enables data from an identification (ID) register containing device identification to be shifted out TDO for viewing. The structure of an ID register should be as follows: (from most significant bit to least significant bit), version (4 bits), part number (16 bits), manufacturer ID (11 bits), and the least significant bit = 1. This allows devices to be polled by a tester for correct part number and version prior to test. This instruction is required for programmable devices. See figure 11-20.

11.2.4.3.7 USERCODE. - Programs ID register data. This instruction is required for programmable components. It allows the user to input an ID code into the ID register from TDI and observe it for validation from TDO. See figure 11-20.



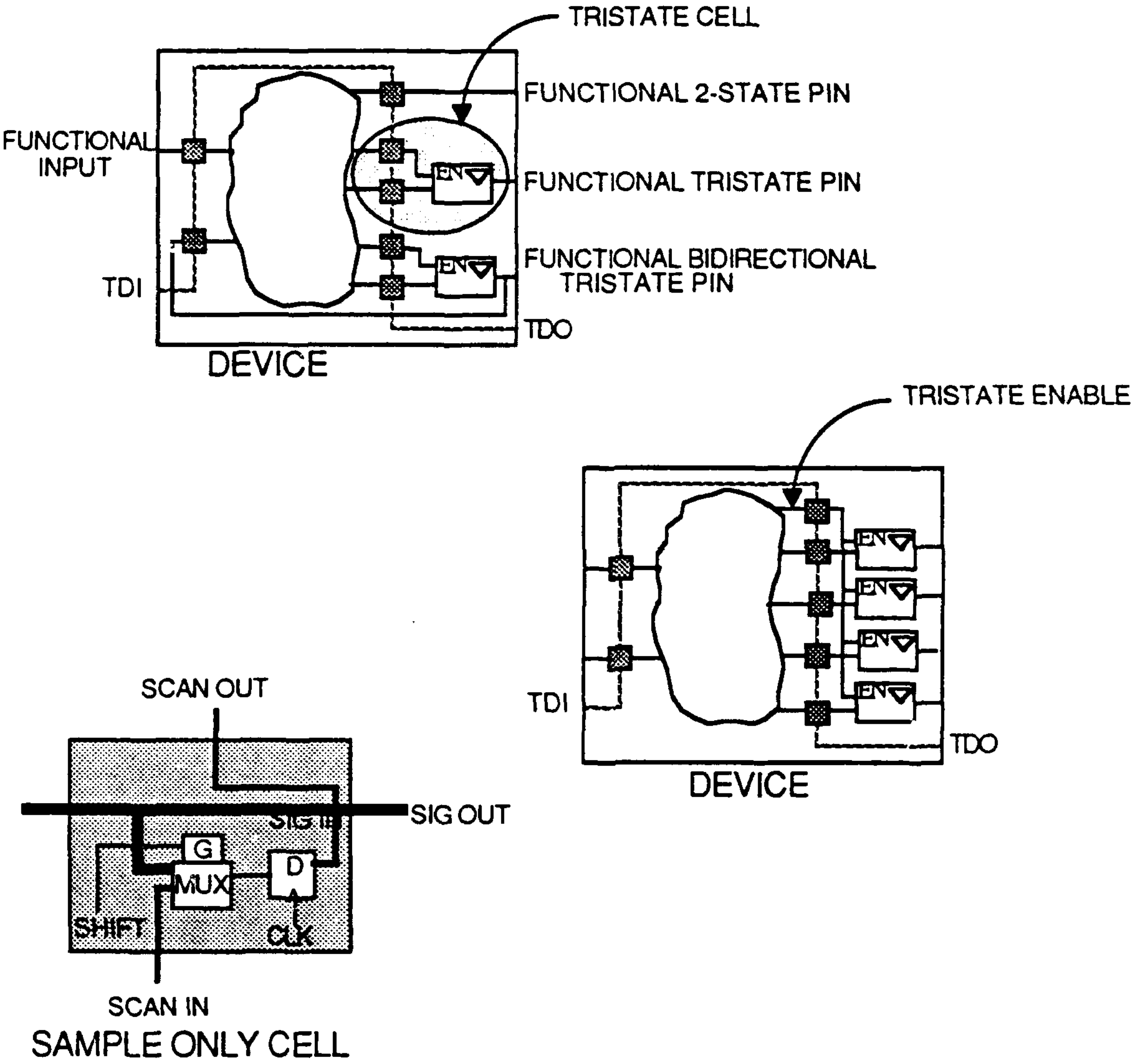
P1149.1 REQUIRED INSTRUCTIONS:
- EXTEST
- BYPASS
- SAMPLE

OPTIONAL INSTRUCTIONS
- RUNBIST
- INTEST
- **IDCODE**
- **USERCODE**

Figure 11-20. USERCODE and IDCODE Instructions

11.2.4.4 Output Cell Requirements. If an output signal of a boundary scan device is bidirectional or tri-stateable during functional operation, boundary scan circuitry must be allocated to control these modes. For either of these two cases a tri-state signal must be controllable by a cell in the device boundary scan chain. Otherwise several boundary scan ICs could have active signals on the same node during test. Several example implementations of devices with bidirectional and tri-state signals are shown in figure 11-21.

11.2.5 Optional Boundary Scan Implementations. The boundary scan examples shown thus far are only a few of the many possible implementations. For instance, if a designer is concerned with a device signal being slowed down by the boundary scan cell MUX, the cell can be designed only to sample and not require a MUX. An example of this cell along with tri-state and bidirectional tri-state cells is shown in figure 11-21.



THIS SYMBOL IMPLIES THE ARCHITECTURE OF A SCAN ⊃ELL SHOWN ON FIGURE 11-12.

Figure 11-21. Sample Boundary Scan Cell Designs

If a user is concerned with a boundary scan chain of cells on a board being too long, the user can design the board as shown in figure 11-22. In the first example, two boundary scan chains are used. Each has a TDI and TDO and both use TMS and CLK for control. In the second example, TDI and TDO are connected to two boundary scan chains in parallel. Each chain is controlled by a separate TMS signal. Also note, that in the first example a boundary scan device with both digital and analog circuitry is shown. In a mixed signal design, cells are placed between analog and digital circuitry.

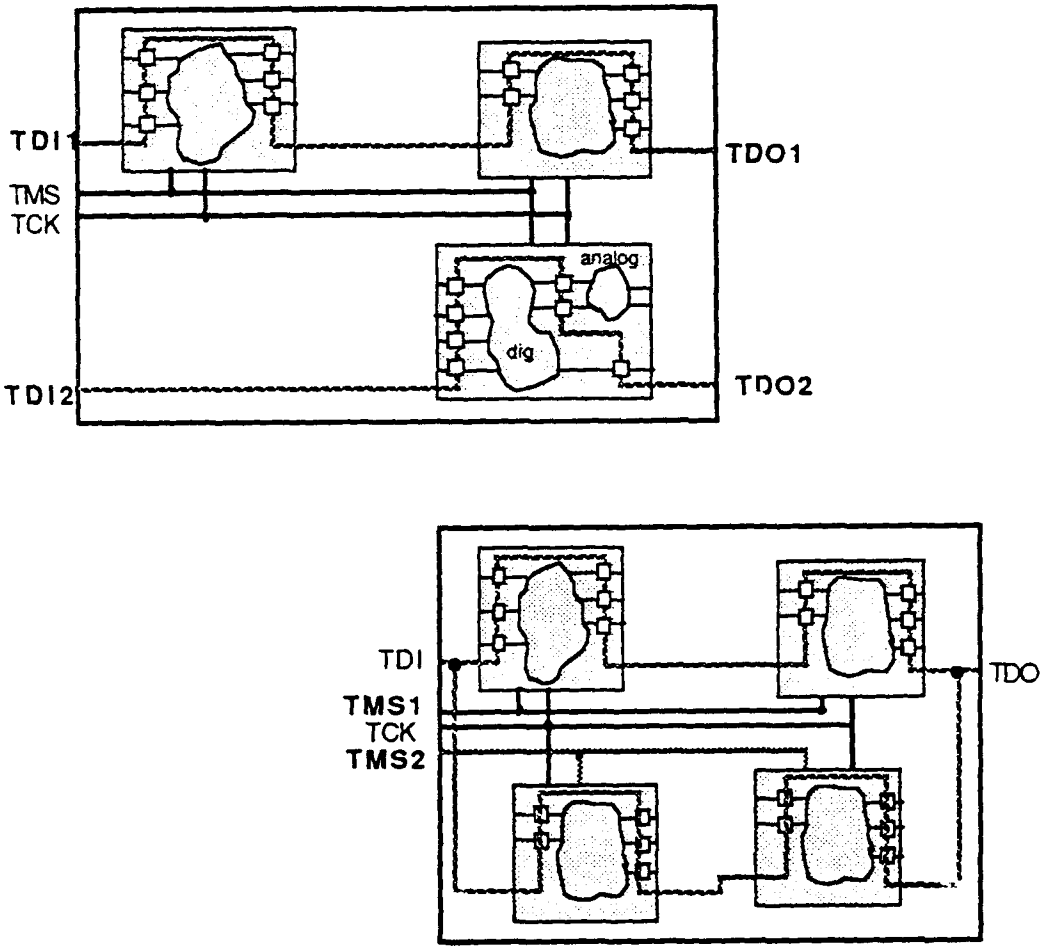


Figure 11-22. Sample Boundary Scan Implementations

One boundary scan implementation used by Texas Instruments was to surround a non-boundary scan device with boundary scan buffer chips. This enabled the ATE to directly control and observe the non-boundary scan device through the buffer chips as if it were designed with boundary scan. This is an example of how boundary scan devices pins can be used as virtual ATE channels to test non-boundary scan logic.

Presently, many companies are designing devices with boundary scan implemented. Some companies (such as Texas Instruments) are working on boundary scan board control chips. Such a chip could be commanded from a system BIT controller to perform a board self-test. Even without using such a chip, the complexity of testability at higher levels is reduced once a board is designed with boundary scan.

11.2.5.1 Mixed Boundary Scan/Scan Designs. Some integrated circuit designs are very complex and require more controllability and observability than boundary scan provides at each device pin. In such a case other scan methods may be implemented along with boundary scan, such as Level Sensitive Scan Design (LSSD) or BILBO. When implemented with boundary scan, these methods can be controlled by the TAP and do not require additional control circuitry.

Often, a device is designed only with scan path for device test but the scan path is of little use during board test. When scan path is used without boundary scan, ATE only has access to internal device registers. The ATE often has no means to control/observe the device inputs and outputs. It can only control internal states and is not very useful during board test. Therefore, for complex circuit designs, it is suggested that both boundary scan and another testability approach like scan path are implemented (unless the design has a thorough BIT).

11.2.5.2 Wafer Scale Implementation. Boundary scan is also an ideal testability approach to reconfigurable wafer-scale integration (WSI). A reconfigurable WSI design consists of many functional chip WSI cells.

Each WSI cell is redundant and used in several parts of the WSI design. Since the WSI cells are redundant, if one WSI cell fails it can be electronically replaced by a similar cell. To implement boundary scan, each WSI cell is designed with boundary scan as an individual device normally would be. Each cell can be tested individually from the boundary scan signals at the four WSI pins. But more importantly, before WSI interconnects between the WSI functional cells are made, each cell can be tested through a standard interface. The interface would require the four boundary scan signals, power, and ground. These signals would be accessible by ATE via pads on each WSI cell. A tester would only require probes to interface to these six standard pads to test every WSI cell individually.

11.2.6 Boundary Scan Benefits. Valuable cost savings will result when boundary scan is used in a design with ASICs. Typically, if a test vendor has to test a board with ASICs, test patterns are not available. The vendor has to develop their own ASIC patterns, which could take over six weeks for each chip. When boundary scan is implemented, the chip manufacturer has to test the boundary scan test logic. This test pattern set could also be used for the board test generation as well. Many ATE companies have realized the possibilities of boundary scan and have begun developing software to automatically generate boundary scan board patterns.

Since boundary scan ATE main concerns are manipulating long serial chains of data on only a few pins, the ATE hardware complexity and computing power requirements are decreased. Some companies are even developing boundary scan ATE controlled by personal computers.

11.2.7 Future Trends. Presently, two boundary scan testability bus enhancements are under development as IEEE standards. 1149.2 is a proposed Extended Serial Digital Signal (ESDS) testability bus standard. It is composed of extra signals that can be added to the 1149.1 signals for an enhanced testability bus. 1149.3 is a proposal Real Time Digital Signal (RTDS) testability bus standard.

11.2.8 Boundary Scan Summary. With the increasing use of SMT devices and new technology developments, access to nodes on a board is becoming very difficult. This makes conventional test costly and undesirable on many designs. Boundary scan 1149.1, is an economical approach to these testability problems. A board tester will require only four serial board I/O connections to have access to every I/O pin on every boundary scan device. (Other connector pins will also be needed to test the runs between the board I/O and boundary scan devices.) Some advantages are as follows:

1. Test software used for chip test can be reused for board test.

2. Board test development is simplified (simulations between boundary scan devices not required).

3. ATE needs only power, ground, and four serial pins to test boundary scan devices. This is a massive reduction in the ATE pin hardware requirements.

4. Interconnects between boundary scan devices and between boundary scan devices and test points (or I/O) can easily be tested.

5. BIT for higher levels is simplified.

6. Data can be sampled through the boundary scan chain without affecting functional operation.

7. ATE computing requirements are decreased from that of conventional test (can run ATE from a personal computer).

8. 1149.1 is an IEEE standard.

There are several penalties that result from implementing boundary scan, but for most designs, the advantages will outweigh the disadvantages. These are:

1. 5-20 percent chip area overhead.

2. 1 ns input signal delay, 1.5 ns output signal delay (through boundary scan cell MUX).

3. Does not functionally test or test at speed. Timing type faults cannot be detected.

4. Not many boundary scan devices on the market as yet.

5. Test software generation and diagnostics are still in the development stage. Long serial test vector chains are not easy to produce or analyze intuitively by the test equipment designer. However, many ATE companies are working on tools to overcome this problem.

6. Front-end design required for chip boundary scan implementation.

NOTE: It is strongly recommended that boundary scan be considered in the design of all custom digital devices.

11.3 Scan/Boundary Scan Testability Guidelines.

(The term scan is used to refer to all forms of scan and boundary scan for the remainder of this section.)

11.3.1 Scan Control Signal Access. If a scan technique is employed in any devices on a module then all scan control lines must be accessible at module connector pins. Every ..struction or scan mode of every scan device must be controllable by the scan control pins or bus brought to connector pins. If the module I/O does not have sufficient pins to carry both functional and scan signals, then a test connector should be added to the module.

A module can contain two levels of scan buses. The lower level bus controls the scan devices and is controlled by a scan control/BIT chip. The higher level bus controls the scan control/BIT chip and interfaces the module to the rest of the system. In such a situation where two scan buses exist, each bus should be accessible at connector pins. The higher level bus will normally be accessible because it is controlled by the system. However, a scan control/BIT chip may only be designed to locate the existence of a module fault and not isolate it to a device. Therefore, since all scan devices must be individually controllable from connector pins, both buses should be accessible at connector pins or through the scan control/BIT chip. As mentioned above, if enough spare I/O connector pins are not available to accommodate the scan buses then a test connector should be added.

11.3.2 Scan/Boundary Scan Electrical Rules. The following scan rules should be employed in scan designs to ease test program generation, reduce scan circuitry interference with functional logic, and to standardize scan designs.

1. Signals being shifted through the scan chain must never invert. If they do invert then fault isolation is greatly complicated.

2. The scan control clock and all scan control signals should be used for test and BIT only and not be used for any functional operations.

3. All scan device tri-stateable signals must be controllable during scan operations. Control should be through a design such as the one in Figure 11-21.

11.3.3 Test Pattern Generation/Scan Support Software. Most scan techniques which do not employ a boundary scan chain are implemented to simplify IC testing but cannot be efficiently used during module test. This is because the IC inputs and outputs are not controllable via the scan (non-boundary scan) chain. Test vectors are simplified since IC registers are controllable, but interactions between ICs need to be simulated in order to generate test patterns. (Data in a scan register of device A must travel through functional circuitry into a register of device B for monitoring).

If boundary scan is used then IC vectors can be directly used on the module. This is because each boundary scan IC is controllable, independent of any IC interconnections. Test patterns used to verify the IC by the manufacturer can be used during module test. Some minor translations of the test patterns are required, but if the design follows a standard (IEEE-STD-1149.1), then translation software should exist for most commercial testers.

If a module contains both boundary scan and non-scan devices, then the non-scan devices can be tested by using the boundary scan devices. Some ATE manufacturers are developing software to automatically generate vectors in this fashion.

11.3.4 Scan Documentation. If a scan technique is employed in a module, then it must be thoroughly documented. Standard scan techniques, such as IEEE-STD-1149.1, are vastly documented and development of a specific documentation package is simplified.

Critical items which need to be documented for modules employing scan devices are:

1. Scan philosophy description.

2. Timing diagrams for each scan control mode.

3. A mapping of each device I/O pin location in the boundary scan chain for each boundary scan mode.

4. Scan path lengths for each possible scan control state.

5. Test pattern generation philosophy - how will test patterns be generated.

6. A table of each scan instruction or mode and the corresponding control word.

SECTION 12. ANALOG TESTABILITY GUIDELINES

12.0 OVERVIEW.

Despite the trend toward digital processing in electronic systems, a significant portion of the electronics will contain analog circuits. This section describes those analog circuits where information is in the form of continuous variations in amplitude, phase, frequency, or waveform.

Some of the fundamental testability concepts such as controllability, observability, and partitioning are the same, but the relative importance of each and the implementation rules can vary. Even within the analog classification there are classes of circuits, Linear, Pulse, High Voltage, High Frequency, etc., which have their own special testability rules and considerations.

The common denominator in such circuits is circuit loading and signal degradation, which inevitably occurs when analog signals are transmitted between the UUT and the test equipment.

Analog and RF circuits require more specialized treatment than other circuits. Special test setups are often required because there are more variables involved than in the digital cases where one must verify a specific pattern/time response to a specific set of inputs. Analog circuit designers must consider variable amplitudes, nonlinearities, phase relations and impedances matching, among other factors. In addition, the circuit designs often include built-in test (BIT) which requires A/D and D/A conversion.

Depending on the application, testability guidelines and implementation can vary due to the diversity of analog designs. The most important point to keep in mind is that the end product must not only work in conjunction with other elements of a system, it must also be capable of being tested in the factory and field.

12.1 General Testability Guidelines.

The following general guidelines apply to almost any analog or hybrid circuit designs, whether it is a substrate, circuit board or system. In common with the guidelines, the basic principles of control, observability and partitioning are of paramount importance.

12.1.1 Controllability. During all levels of test it is necessary to be able to easily control the function or modes of an analog circuit. The degree of difficulty is usually not as great as it is with digital circuits, but the major considerations are as follows:

1. Any ON/OFF control lines for switching, mode control, etc., should use one standard interface level. (TTL compatible is preferred).

2. Avoid complex or long digital control sequences. Decode logic can be re-partitioned onto a digital board and the switch controls presented at the analog board I/O. Analog ATE usually does not have sophisticated digital control compatibility.

3. Any long time constants should be controllable so that they can be tested quickly.

4. Do not use small control voltages at the UUT I/O pins. Signal interfaces should be designed to be easily and accurately reproducible and to avoid stray pick-up from typically noisy ATE systems (figure 12-1).

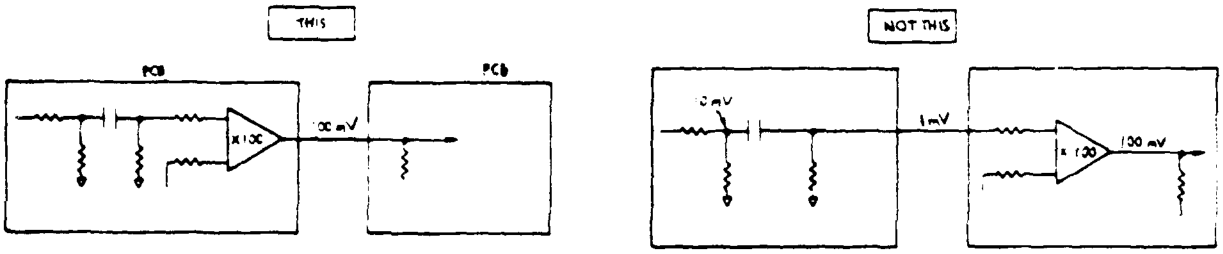


Figure 12-1. UUT I/O Pin Voltage Level

5. Test pins should be used at the edge connector to circumvent logic nets or high gain circuits and get directly to analog control pins. These test points also help improve the diagnostic process when the control circuitry fails. (See figure 12-2).

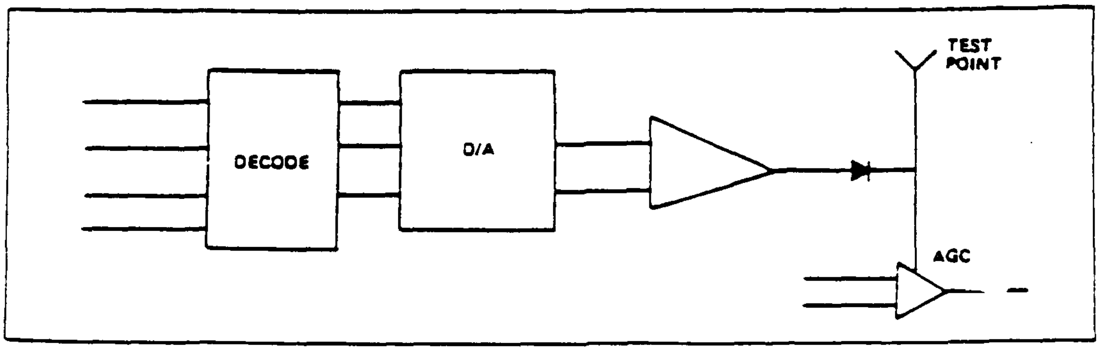


Figure 12-2. Use of Test Points

6. In general, any test point should be analyzed for its potential as a controlling input and for partitioning the circuit into functional blocks.

7. Break feedback loops during test and debug operations. Open-loop testing is preferred for preliminary circuit tests and is preferable for fault isolation. Final tests should include a thorough exercise of closed loops. Implementation of this requirement may use an analog switch or multiplexer controlled by the ATE or BITE. Any implementation that allows electrical control of the feedback loop is preferred over mechanical switches or jumpers that need manual intervention.

12.1.2 Observability. In an analog circuit, observability may mean physical accessibility to a circuit node as it does in a digital circuit (section 7.2). It can also mean compatibility which is related to the capability of the test equipment to acquire the specified data with the required resolution and accuracy.

An analog device or circuit which performs a function, such as an op amp or filter, is referred to as an analog macro. Test points should exist at macro boundaries and individual macros should follow general partitioning, controllability, and observability rules.

12.1.2.1 Accessibility. Accessibility to circuit functions that may be buried in the middle of a board can be accomplished via edge connector test pins or via analog switch (multiplexer) circuitry that can also frequently be used as part of the BIT circuitry in the system application.

Care must be taken to ensure that test points do not cause system or test problems of their own. Adequate isolation must be provided so that stray board or tester capacitance does not affect the circuit. The location of the test point and the type of buffer circuitry provided should be designed to result in easily measured signals being presented at the module pins. Test points beyond those required by test specifications can be very useful. The designer should consider potential failure modes, failure frequency and diagnostic techniques in the selection of test point locations.

12.1.2.1.1 Multiplexing Test Points. Most electronic packaging schemes impose pin limitations which may preclude direct access to a sufficient number of test points for the required level of fault isolation. Many designers, when faced with pin limitations, reduce the number of test points to make the circuit fit the package. There is seldom any consideration given to combining test point signals. The result is often a design which is incompatible with automatic test because there is insufficient access for fault isolation.

Figure 12-3 illustrates a method of achieving accessibility by combining, rather than eliminating, test points. In this example, a resistor summing network is used to combine two signals of opposite polarity. Resistor ratios can be selected so that the polarity of the test signal indicates which amplifier is faulty. The only requirements for combining test points is that at least one measurable characteristic of the combined signal is a function of each input signal. AC components of the output test signal are proportional to two different input signals.

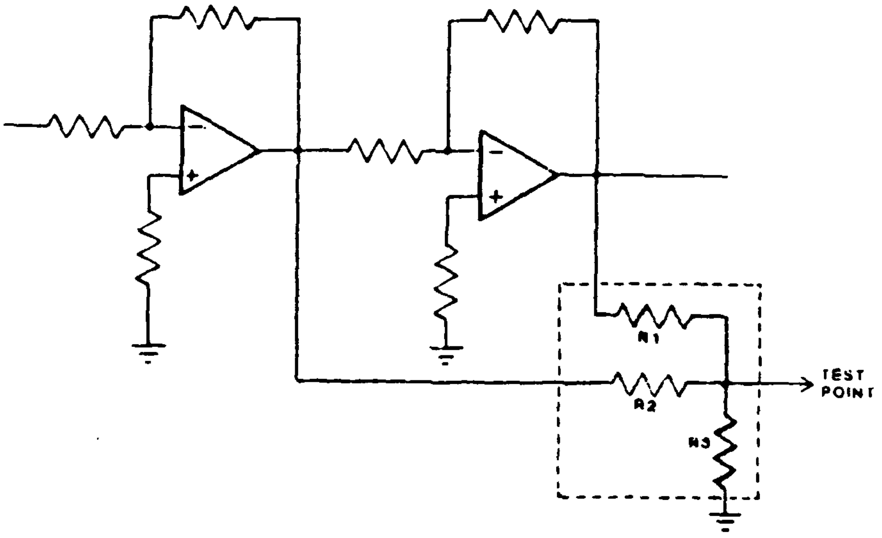


Figure 12-3. Resistive Summing Network

Large numbers of signals can be merged onto one test point pin by using IC analog multiplexers. IC multiplexers can also solve the problem for circuit nodes of widely varying voltage levels or sinusoidal signals that could not be combined as shown in figure 12-3. The multiplexer is the best general approach for the combination of test points. (See figure 12-4). When combined with a sample/hold circuit card A/D conversion, this can provide a very powerful BITE tool in conjunction with microprocessor control.

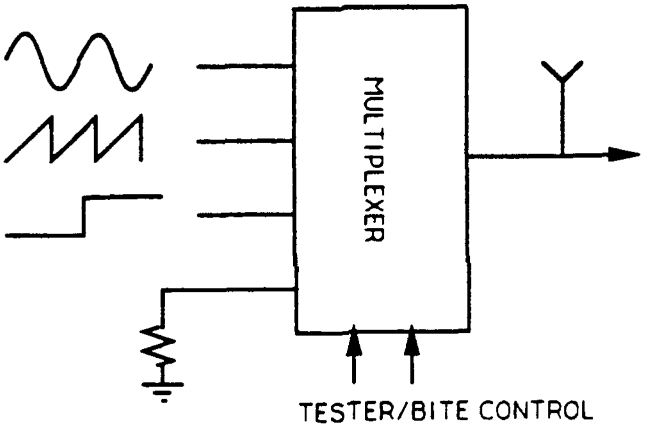


Figure 12-4. Combing Test Points

12.1.2.1.2 'Lowest Wins'/Wired-OR Circuits. A 'Lowest Wins' type circuit using a wired-OR configuration is often used to combine various status or control lines. However, if the circuit is directly wired then locating a failed component becomes difficult, (similar to digital wired-OR logic - see section 7). Simply adding series diodes to the circuit results in a more testable circuit with better fault resolurion. (see figure 12-5).

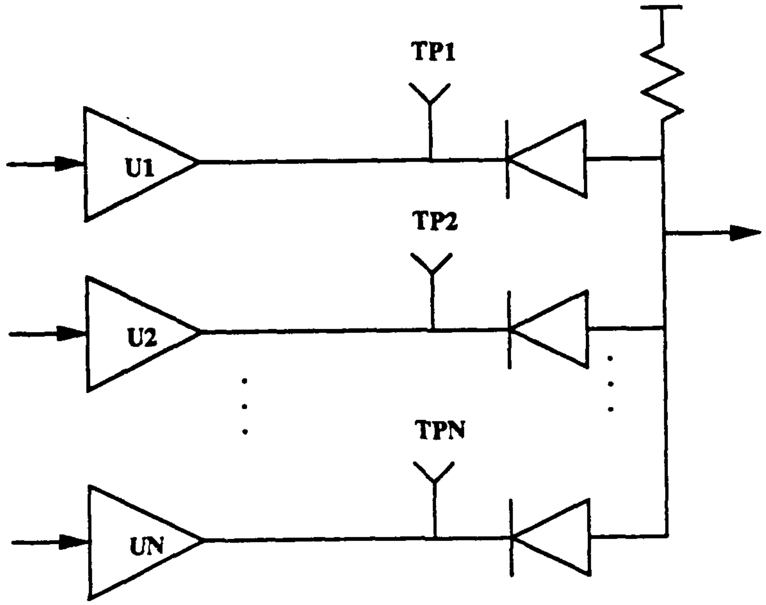


Figure 12-5. Testable 'Lowest Wins'/Wired-OR Design

12.1.2.2 Accessibility Design Guidelines. The following analog test point guidelines should be considered in designing new products:

1. Test points for test signal injection and signal observation should be included at each major circuit function not accessible from the edge connector.

2. Test points should provide a reasonable and useful facsimile of the signal being monitored. Check for correct impedance matching.

3. Ground points or turrets should be provided for the convenient connection of probe returns.

4. On plug-in modules, test points are more accessible to ATE if they are built into the I/O connector. Use of an empty IC socket for test points is a good alternate choice if sufficient edge pins are unavailable.

5. A connector that is larger than the minimum size required for system functions should be chosen so that there will be room for test points.

6. Another possible solution to the test access problem in low frequency analog circuits is the use of separate "test only" connectors. A test connector mounted on a different edge (figure 12-6) provides extra pin capacity.

   Test connectors should be a different connector type than the I/O connector or be keyed so that the test connector cannot be accidentally plugge‹ into the I/O connector port.

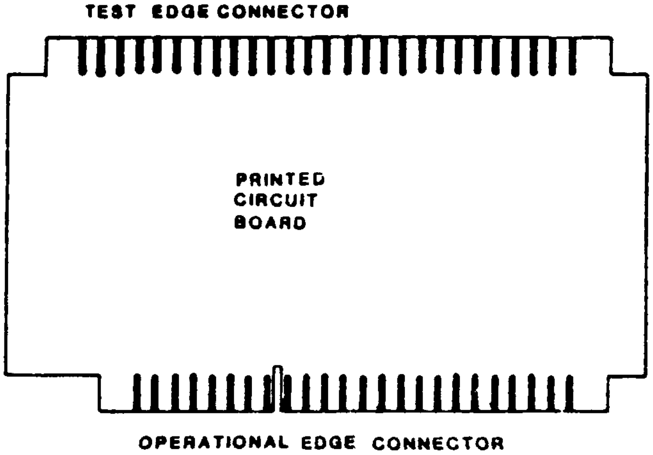


Figure 12-6. Test Connector Mounted On a Different Edge

7. Circuit pads for manual probing are useful for troubleshooting, but are not compatible with automated testing unless a simple interface device can be supplied to contact these pads, thereby avoiding manual intervention during test execution. A bed-of-nails fixture is a possible solution. Masking of test pads from conformal coat is a necessity.

8. Ideally, every active device output should have a test point available.

9. Test points can be important on packaged, replaceable microcircuits or modules as they may provide the only means to isolate a fault to that module once it is installed in a circuit.

10. Test points should never be allowed to represent hazardous voltages or potentially high current levels. Appropriate techniques are spelled out in MIL-STD-454.

11. For RF and IF signals, test points should be compatible with common impedances and connector types (50, 75 ohm, BNC, or SMA connectors).

12. Test points should not be allowed to load down the signal or degrade performance when connected to a measuring device (meter, etc.).

12.1.2.3 Compatibility. Making an analog signal accessible to the ATE system is only part of the observability problem. The ability of the ATE to detect, measure and discriminate whether a parameter passes or fails is equally important. The specifications and tolerances on the signal parameters must be compatible with the measurement or signal generation characteristics of available ATE.

When the design is an addition or change to a system already in production, it is extremely important to consider that program's ATE capabilities. New ATE systems or modifications to existing ones can be very expensive, and acquisition times are quite long. Adding a circuit to an existing design with a new frequency range or very tight measurement tolerances can have a significant effect on the life cycle cost of a product.

On new programs that will have a new generation of factory ATE, it is important to confer with the production test equipment designers and test engineers. Verification that the proposed specifications, tolerances and functions can be measured on production test equipment if required. If signals can not be measured with the available test equipment then the signals are considered complex and indirect means have to be developed to measure them.

12.1.2.3.1 Loading and Buffers. Ensure that test points/outputs can drive additional capacitance/lead length for use with extenders and test equipment.

When low-frequency analog circuits are tested on ATE, it is the distributed capacitive load that is generally the most significant interface characteristic. Typically, this load is equivalent to a 1000 to 2000 pF capacitor at the output of the UUT. This capacitance is typically distributed as follows:

•	External test cable:	300 pF
•	ATE interface device:	250 pF (each path)
•	Internal ATE configuration cabling:	250 to 1400 pF

Therefore, each and every test point cabled to the ATE will be loaded with roughly 500 pF, whereas the particular test point under observation will have perhaps twice this amount.

The reactance chart in figure 12-7 can be used to estimate the impedance represented by this capacitive load at various frequencies. A capacitance of 1000 pF at 10 kHz, for example, has a reactance of 16 kW load at the UUT test point connector. Clearly the effects of this load cannot be neglected in the circuit design and in the specification of nominal test values and tolerances.

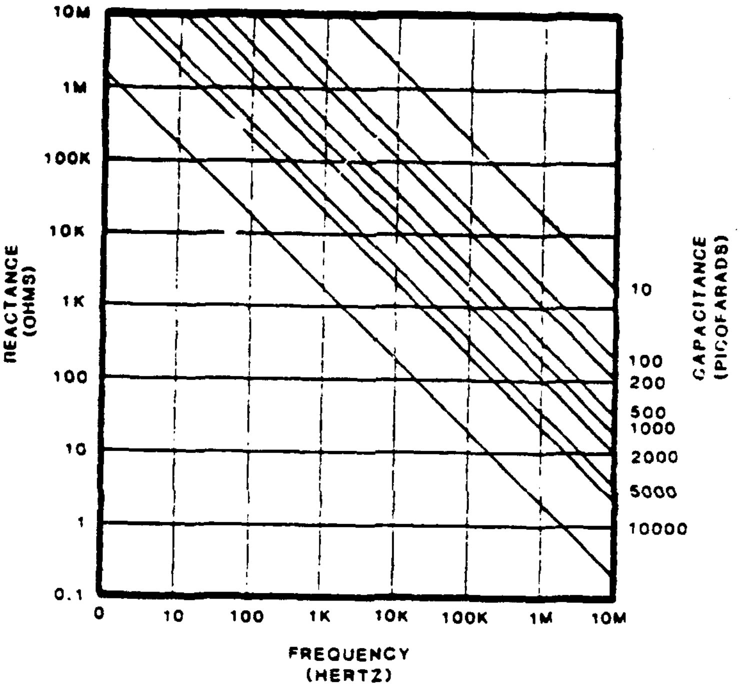


Figure 12-7. Reactance Chart

Test points must be located at circuit nodes which are insensitive to the load imposed by the test cables. In a common emitter amplifier, for example, a small unbypassed emitter resistor provides a good test signal source which is relatively insensitive to loading and to injected noise (see figure 12-8).

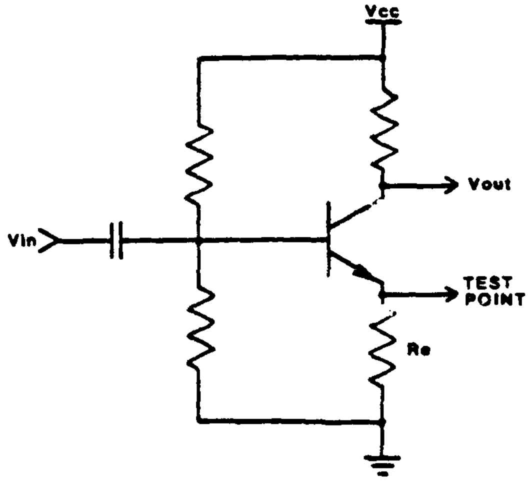


Figure 12-8. Common Emitter Amplifier Test Point

Operational amplifiers configured as voltage followers provide a good test signal source. There are many advantages to this application, as opposed to the emitter follower amplifier. Many of these "MIL-approved" devices are internally short circuit protected, and some are compensated for unity gain operation. They can operate in a bipolar mode and the output of a unity gain buffer will be within a few millivolts of the input.

When operational amplifiers or emitter followers are used, they must be stable under required loading conditions presented by the ATE or the circuit to be injected with a signal. An emitter follower can oscillate when connected to capacitive loads greater than 200 pF, and capacitive loading can add a phase shift to the feedback loop of an operational amplifier, possibly causing peaking, ringing and even oscillations at low amplifier gains.

To prevent the undesirable effects of capacitance loading, it is sometimes necessary to decouple the load from the amplifier, which is done in an emitter follower by placing a small resistor in series with its base or the load. With operational amplifier circuits the capacitive effect can be minimized by:

1. Choosing an amplifier with low output impedance.

2. Adding a buffer stage (op-amp, transistor, or FET).

3. Using the phase compensation scheme shown in figure 12-9.

Use of dual or quad op-amp ICs helps to keep the cost of implementing buffer stages at a minimum.

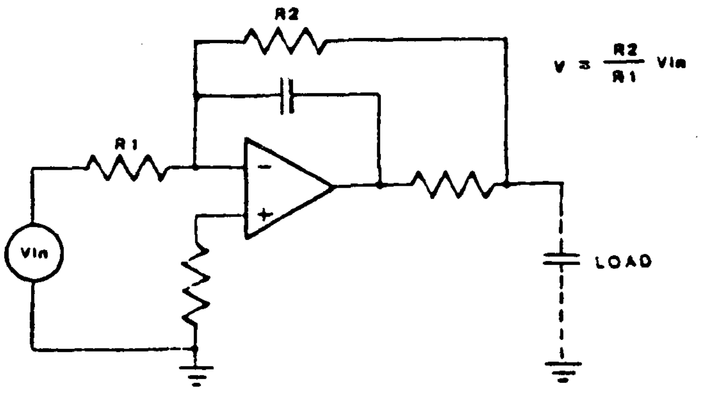


Figure 12-9. Phase Compensation Scheme

A decision must be made whether to include active buffers in a UUT or in the test adapter design. When added to the UUT, the weight and overall costs are increased, but the test interface adapter requirements are reduced. In addition, circuits within a UUT must undergo all the severe environmental stresses required of the equipment, which would not be a requirement if the circuits were located in the interface design. The tradeoff is one of reliability and cost effectiveness. With today's technology in MSI and LSI, circuit inclusion in the UUT is achievable and provides additional test capability that enhances the BIT function.

When the equipment uses discrete rather than integrated circuitry, it is usually more cost-effective to place these active circuits in the interface design. Comprehensive test features can be built into the circuits within an interface adapter. However, these added circuits can customize and thus limit the use of the interface adapter with other types of UUTs.

Active circuits added to a design have one function: to improve testability. Therefore, they must be added in a way that does not introduce new testability problems. Clearly, when these circuits are added in the form of additional component parts, they can have an adverse effect on maintainability at the next level of assembly if they are utilized as part of the circuit function (such as BIT).

12.1.3 Partitioning Analog Circuits. As noted in the two preceding sections, partitioning can be used to effectively improve the controllability and observability of a circuit. Separating control logic from analog circuits and breaking up circuits so that the important test points appear at edge connector pins are fundamental testability techniques. There are a number of additional considerations that are equally important. When partitioning a system, these rules should be followed:

1. Partitioning Analog and Digital Circuits - Separate analog and digital circuits into different boards such that the resulting modules are as purely analog or digital as possible. Make the remaining mixed analog/digital circuitry into separate parallel functions, independently accessible from the I/O connector pins. Mixing analog and digital circuitry puts extra demands on test systems and test support personnel; both are usually specialized in either analog or digital. Mixed circuits are unnecessarily difficult to troubleshoot, and even computer-aided fault isolation usually cannot handle the mix. Mixed boards often need to be tested on two separate test stations, an unnecessary cost driver.

2. Partition Diverse Analog Functions - For similar reasons, diverse analog functions, Linear, Pulse, High Voltage, High Frequency, etc., should be self-contained on one module. Avoiding the expense of multi-insertions on different testers and multi-skilled test technicians is the goal. Consult with the ATE designers or production test engineers to determine what mix of circuitry can be accommodated on available ATE.

3. Include a Complete Circuit Function on a Single Module - Avoid scattering portions of a circuit function, such as an amplifier, onto multiple circuit cards. Specifications are easier to develop and control, and troubleshooting is much easier when a circuit is a recognizable entity.

4. Analog Functional Modularity - Functional modularity can be more easily achieved by using integrated hybrid and monolithic circuits. Many of these integrated circuits are MIL-approved parts, and others are processed and inspected in such a way that MIL-qualification is readily obtained. Some typical examples of integrated devices are operational amplifiers, V/F converters, D/A converters, A/D converters, phase lock loops, crystal filters, oscillators, RF amplifiers, sample and holds (S/H), etc. Functional modularity in analog circuits can significantly reduce the number of test points required for fault isolation in assemblies by reducing maintenance to direct replacement of the faulty circuit module.

   This also has a distinct advantage over discrete circuitry in that component ambiguity group size is reduced when isolating faults. Recent Government contracts have tightly specified BITE and maintenance test requirements to keep the fault ambiguity group small.

5. Partition to Reduce Adjustables - Location of a complete circuit function on a single board can have the effect of eliminating some adjustable/ selectable components. Another consideration may be making a single adjustment at subsystem or system level to eliminate multiple adjustables on the lower level assemblies, such as Line Replaceable Units (LRUs) and Shop Replaceable Units (SRUs).

12.1.4 Specifications and Tolerances. The types of parameters specified and the tolerances placed on them can have a tremendous impact on the cost, producibility, and testability of analog electronics. The need to specify many parameters and tight tolerances at LRU levels to ensure that system performance will be achieved cannot be overlooked. Frequently, lower level test specifications are incomplete or contain unrealistic tolerances. In some instances, a lack of time available to perform a complete set of accurate tolerance calculations is the reason and this results in specs that are expedient rather than necessary. Under these conditions, the approach has been to specify tighter tolerances with the hope that the unit would function in the next higher assembly. Increased cost due to low production yields and the labor associated with the adjustable circuits required to meet the tight tolerances are the result. The widespread availability of CAD now makes it practical to quickly perform tolerance calculations and design analysis in the early phases of a program and minimize these costs. Some guidelines are listed here:

1. Specification Consistency - The designer should be sure that the specifications at each level of buildup are supported by lower level specifications (down to and including component and "black boxes"), derated to account for circuit interactions, cables, and stray RLC (resistance, inductance, and capacitance) factors. A worst-case analysis is necessary to ensure that an out-of-spec condition can be detected and that false alarms are minimized.

2. Error Budgets - Distributing a portion of the allowable system/subsystem error down to lower level assemblies helps ensure high production yields and allows the board designer to select economical, testable circuits with a minimum of adjustments required.

3. Component Specifications - Inherent characteristics of a particular vendor's component should not be depended upon for operation of a circuit. All critical parameters should be specified on the Specification Control Drawing (SCD) so that vendor process changes or substitution of a second source vendor's component will not affect circuit operation.

4. Environmental Considerations - Component specification derating over temperature or other environments must be taken seriously. Applications test of a small sample is no guarantee that eventual production yields will not be affected. SRU, LRU, and system specifications must be derated consistent with component performance. In nearly all cases, room ambient performance must be specified to tighter tolerances than temperature performance. The only exceptions are in cases where there is no thermal drift associated with a parameter or where tighter measurements are not possible. The direction of thermal drift should also be taken into account to allow accurate placement of the tolerance window. If this procedure is not followed, units that marginally pass at

ambient will eventually fail at temperature. The resulting troubleshooting analysis and Engineering Change Order (ECO) activity is very expensive.

5. Test Equipment Capabilities - The specifications on a circuit must be consistent with the capability of production or field support ATE to provide the required stimulus and measurement. Test requirement specifications normally specify tolerances on performance parameters without allowing for test measurement errors. Test equipment should have an accuracy ratio of ten to one (10:1), where accuracy ratio is defined as the specification limit/measurement system accuracy. Measurement accuracies should be at least four times better than the specification requirements so that customer certification of factory test stations can be obtained. Specification limits need to be adjusted to compensate for measurement errors if the test equipment does not have an acceptable accuracy ratio (about 4:1). Test tolerances can be calculated as a Root Sum of Squares (RSS) when the error sources are statistically independent, normally distributed and the same number of standard deviations are used. For example:

$$T = \sqrt{TU^2 + TT^2}$$

where

TU = UUT tolerance as defined by the performance spec.

TT = Test equipment system measurement accuracy.

T = Adjusted specification limit.

To prevent false test rejects due to test equipment inaccuracy the test specification limit should be relaxed using the preceding formula. If the spec limit is critical and cannot be relaxed without impacting the yield at higher levels of assembly, then the test limit should be tightened (with an accompanying decrease in yield at the lower level) using the following:

$$T = \sqrt{TU^2 - TT^2}$$

The effects of test station loading on circuits should also be considered in the specifications. Communication between the design engineer and the production test equipment designers is very important to resolve these issues prior to test.

6. Test Time - Specifications of numerous parameters, many frequency points etc., has a significant impact on product cost and the capacity of the factory test equipment. Testing should be reduced to the minimum required to ensure a high yield probability at next level or system level. Testing decisions are usually based on economics and product experience. The cost of obtaining the data at low levels must be balanced against the probability of a failures at higher levels. A total system review of the specification pyramid is required.

7. 100-Percent Test Versus Sample and Design Test - Parameters that are inherent to the basic design, and are unlikely to vary because process controls and vendor specifications control them, should be identified as Design Tests. This category of tests should be performed only at the start of a production run. Other parameters that, due to wide tolerances, favorable production test experience, or that are of a lot-related nature, should be identified as Sample Tests. A 100-percent test philosophy must be applied to basic function circuit parameters with a failure history and functions or parameters that cannot be measured at higher levels. Sample versus 100-percent test of parameters that can be measured at higher levels is an economic decision that can be based on experience.

12.1.5 Adjustables/Select-On-Test. If at all possible, specifications should be budgeted or relaxed to avoid the need for adjustable, tunable or selectable components. Test times and high operator skill level requirements make these circuits very expensive to produce, and they frequently become production bottlenecks.

Adjustables (sometimes referred to as nominals) may be required under certain circumstances, such as when system level testing results in the changing of a modules requirements. However, as a goal, all system level adjustments should be automatic (digitally controlled or analog AGC for example). If it is determined that an adjustment is necessary, then the primary concern is to make the adjustment process straightforward and easy to perform during all test phases.

The following guidelines should be followed if an adjustment is required:

1. Use a nominal component when the adjustment is independent of other adjustments or can be determined in a straightforward manner. For example, a nominal should be used to set threshold or gain levels.

2. Avoid inserting nominal components directly in the signal path.

3. Do not place nominals on substrates.

4. Specify the resolution between values of selectables which are adequate for the application. It should not be so broad that the correct value of component cannot be selected, nor so fine that several of the same value of component must be tried to satisfy the requirement.

5. If nominals are used, bifurcated or turret terminals should be provided so that the components can be installed at the test station, thus reducing the amount of handling.

6. If possible, adjustables should be avoided altogether by the use of digital gain control via D/A Converters or digital attenuators (see figure 12-10).

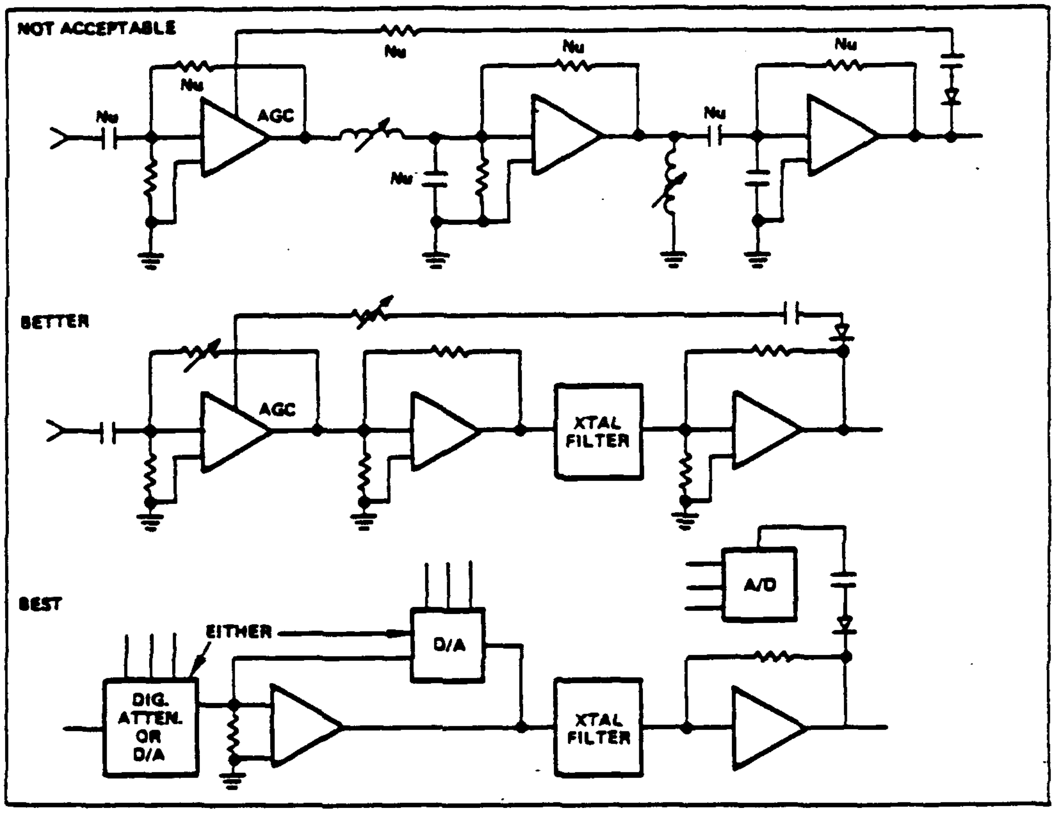


Figure 12-10. Minimizing Adjustables

7. The use of multiple tuned elements directly on circuit cards should be avoided. The designer should attempt to use purchased filter/oscillator modules.

8. All elements of a tuned amplifier and filter chain should be placed on a single card if possible, and a single adjustable component used to adjust gain or AGC. If all circuitry does not fit on a single card, it should be set up so that there is only one adjustable at the next higher level.

9. Variable components should be used instead of selected nominal components to accomplish trimming or tuning of circuits if the program allows. Expensive rework cycles in production will be eliminated and the parts inventory will be reduced.

10. Include adequate test points to help predict the final values required, thus minimizing the number of presentations of the hardware to the test station. The analysis used to calculate the range and granularity for the application should be supplied to production as an aid in nominal selection.

11. Minimize the interaction between any two or more adjustables. Test time increases exponentially with the number of adjustable items in series.

12. Use continuously variable components when several adjustments are interdependent. For example, tunable filters should always use variable components instead of nominals. The only exception is where one variable must be set accurately in order to tune the filter using the other components.

Adjustments at the module level are intended to be set at the factory and not changed in the field. Tampering with settings, vibration effects and the reduced reliability of adjustables are potential problems to be considered.

It must be emphasized that the decision to use module level adjustments requires an analysis of the production environment which involves trade-offs between assembly, test, yield, cost, component delivery and performance. Components of appropriate precision rated at their "end-of-life" tolerance for worst case environments can be used in place of adjustments. Programmable adjustments with digital techniques can also be utilized.

The use of any adjustables should be carefully scrutinized during the testability portion of the Design Review, and very strong production cost justification should be required.

12.2 Specific Analog Design-to-Test Guidelines.

The following subsections contain more specific testability guidelines for various types of analog circuits. Microwave and MMIC testability are dealt with as separate topics (see section 13).

12.2.1 Low Frequency Linear and Pulse Circuits.

12.2.1.1 Hardware Design Guidelines for Low Frequency and Passive Circuits.

1. Adjustments. Minimize the use of adjustments requiring trim-pots, trimmer capacitors, etc. These components extend test time and require interactive testing and verification of range adjustments. During operation such components are sensitive to vibration, drift and tweaking, which lead to downtime. Interactive adjustments on different assemblies should be minimized. In place of adjustments, design components of appropriate precision and rated at their end-of-life tolerance for worst case environments, or utilize programmable adjustments with digital techniques (see para 12.1.5).

2. Relays - Minimize the use of relays because of their inherent unreliability.

3. Damage immunity. In analog circuits, the I/O assembly should be desensitized to testing mishaps. Designs should be immune to the transients, potential shorts, and open circuits, which can be encountered through testing, and no test point should be excessively vulnerable. The design should also be immune to the sequence of application and removal of power. To preclude the effect of ATE power supply noise, it should be specified and controlled as required or adequately buffered.

4. Voltage regulators. Voltage regulator oscillation is a very common problem, which is very difficult to detect on ATE and diagnose at production test. Switching regulators should be used for power applications if possible. Linear regulators must be avoided or carefully stabilized. Thermally protected regulators are preferred to the foldback type. Current foldback is very difficult and time consuming to measure and is susceptible to transients in operation.

5. Signal Interfaces. Design interfaces so that inputs, outputs and test points, have large, robust signals that are easily and accurately measurable or producible. This will minimize noise problems in the designed unit.

12.2.1.2 Specification Guidelines for Low Frequency Active and Passive Circuits The following measurements are difficult to achieve on ATE and should be avoided by use of a Sample Test or Design Test philosophy. Use of design approaches that exceed specification requirements by a wide margin (if this can be achieved with reasonably priced components) is another possible method. Margins can also be widened by reallocation of system budgets. These types of tests should be avoided:

1. Pulse rise/fall times

2. Slew rate

3. Pulse overshoot, undershoot and ringing. If it must be specified, define carefully using a pictorial representation.

4. Triangle or ramp waveform linearity

5. Tight gain versus frequency measurements on tuned circuits.

6. Allow as much latitude as possible on filter shapes.

7. Gain ripple. Define carefully, if it must be specified, using a pictorial representation.

8. Absolute pulse voltage.

9. Phase shift to < 5 degrees tolerance.

10. Gain to < 0.2 dB.

12.2.2 Data Conversion Circuits.

12.2.2.1 Design Guidelines. Testability guidelines for data conversion circuits are as follows:

1. Direct access should be provided to the data conversion device I/O and control pins. A bus structure, as shown in figure 12-11a or a loop through the I/O pins as shown in figure 12-11b, are both acceptable, with figure 12-11b the preferred approach, provided that sufficient I/O connector pins are available. With these arrangements, the analog, A/D and logic circuits can each be tested and fault-diagnosed independently. Without the test points shown, the circuit is untestable on standard ATE systems and is very difficult to troubleshoot.

2. If glitches or spikes occur in voltage-to-digital conversions and vice versa, current type conversions should be tried instead, as these tend to be smoother in operation and easier to test.

3. If there is any probability of a change in the signal during the conversion period, a Sample and Hold technique should be used to avoid digital miscounts. The sample and hold control line should be accessible to the ATE.

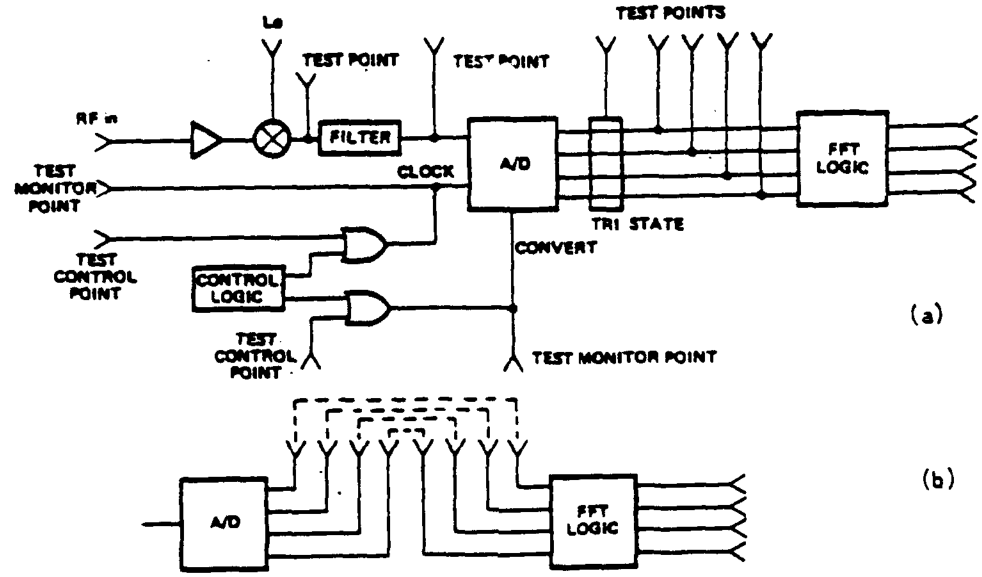


Figure 12-11. Test Point Placement For Data Conversion Devices

12.2.2.2 Specification Guidelines for Data Conversion Circuits. The parameters listed are difficult to measure on ATE and should be avoided by a use of a Sample or Design Test philosophy. Use of design approaches that exceed specification requirements by a wide margin (if achievable with reasonably priced components) is another possible approach (e.g., using a 12-bit converter when a 10-bit would suffice). Margins may also be widened by re-allocation of system error budgets and tolerances.

1. Droop testing of Sample/Hold devices.
2. "Glitch" (transition noise) testing of D/As.
3. Settling time of D/As.
4. Conversion time of A/Ds.

5. Linearity and accuracy on 100 percent of the steps on A/Ds. These tests are not as difficult to perform on D/As if a reference DAC is used and only major carry points are measured. If necessary, the slope or gain of the UUT A/D, and not the absolute value, should be measured, or the slope should be specified tight and the absolute value loose to accommodate any test equipment offsets. Testing should be conducted at clock rate or system update rate if speed is critical and only if the design margin is small.

6. End-to-end signal processing testing, such as FFT testing, should be deferred to the higher level where the UUT digital processor becomes available to process data. A pure logic test, analog test, and converter test should suffice at the SRU level if the system is properly partitioned.

12.2.3 Monitoring and Control Circuits. Testability guidelines for monitoring and co^ntrol circuits are as follows:

1. Metering, display, or LED circuits are much easier to test if the display drive lines are accessible to the ATE system.

2. RF meters in drive-critical circuits should be placed as close as possible to the driver element for detection of feed line and VSWR problems.

3. Controls and indicators should be contained on an assembly separate from the one that contains the electronic circuits. This permits fully automatic test on ATE of the electronic part, and manual test of switches and indicators with standard general purpose instruments (an ohmmeter is usually sufficient).

4. Unless otherwise specified in the equipment specification, meters should have provision for overload bypass or alternate protection to eliminate high voltage potential or current at the terminals in the event of meter failure. (See section 14).

5. Control switches that are an integral part of an electronic assembly should have a test position that permits automatic remote control of the electronic circuits by the ATE station.

6. Any transducer electrical interface should be accessible to the ATE system or BITE. This includes any conversion of electrical energy to or from the following energy forms:

   a. Optical (see section 16).
   b. Audible.
   c. Mechanical (position, speed, pressure, etc.) (see section 17).
   d. Magnetic.

   (This covers such varied transducers as loudspeakers, CRTs, accelerometers, etc.)

SECTION 13. HIGH FREQUENCY TESTABILITY GUIDELINES

13.0 OVERVIEW.

This section presents guidelines and recommendations for circuit designs with high frequency signals from 50 MHz to 300 GHz and beyond. Radio Frequency (RF) is usually referred to frequencies which range from 50 MHz to 300 MHz. Microwave and millimeter wave frequencies range from 300 MHz to 300 GHz. Testability rules for frequencies in the thousands of GigaHertz range are included in section 16 - Electro-Optics. Circuits which are high frequency need to follow the general technology guidelines contained in earlier sections, but special conditions need to be maintained for high frequency modules.

13.1 High Frequency Linear and Pulse Circuit Guidelines.

13.1.1 Hardware Design Guidelines for High Frequency Active and Passive Circuits.

Design guidelines for high frequency circuits are as follows:

1. Convert to a 50-ohm impedance at all test point and I/O ports. Adequate buffering should be provided to account for reasonable expected mismatches typically found with test fixtures or test equipment. (Or clearly specify the allowable mismatch.)

2. Resistive attenuators are the most commonly used matching networks where wide bandwidths are required. The resistors in the network must have low series inductance and shunt capacitance with maximum permissible values determined by the desired frequency range. A typical impedance-matching network is shown in figure 13-1.

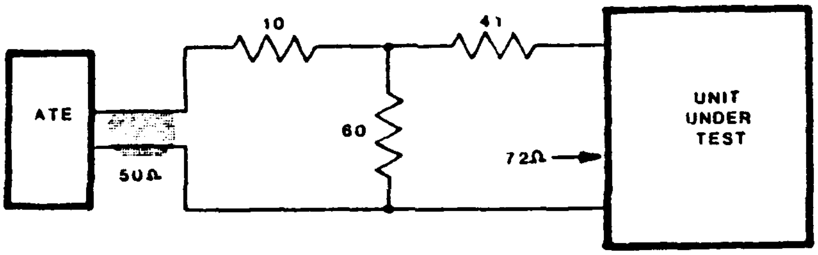


Figure 13-1. Typical Impedance Matching Network

3. For those applications where a single frequency or narrow band frequencies are involved, reactive LC matching networks can be used (figure 13-2).

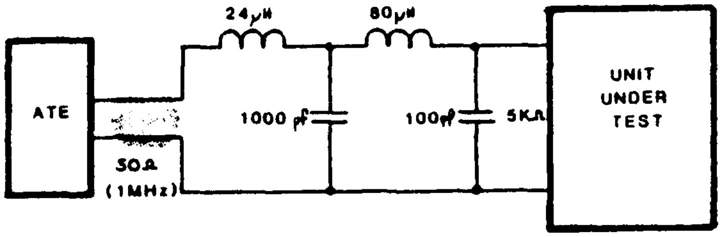


Figure 13-2. Reactive LC Matching Networks

4. The methods and techniques for designing impedance-matching networks should be familiar to most circuit designers and can be found in standard engineering handbooks. Caution should be exercised because the standard handbook variety LC matching circuit is designed for maximum power transfer, which is desirable at the inputs and outputs of a UUT. Matching networks at the intermediate (fault isolati^n) test points, however, must be designed for minimum disturbance to the circuit under test; thus the power withdrawn from the circuit must be minimized and the matching circuit must not disturb the UUT by the open stub that is present when a test point is not switched to a response monitor instrument.

   In a typical system, only one measurement is taken at a time. The response monitor inputs to the ATE are terminated in characteristic impedance (Z0) only while a measurement is being maue. At all other times, the line from a UUT test point could be terminated at an open switch contact on a switching unit. The effects of these open stubs on the circuit under test cannot be neglected. Matching circuiis within the UUT must isolate critically tuned circuits from the detuning effect of the reactive impedance of these stubs or must be compensated for in the interface design.

5. Two commonly used techniques for test point isolation are shown in figure 13-3. The number of turns in the test point winding of the RF transformer is selected to minimize the effect of the ATE stub on the circuit under test while supplying a measurable signal amplitude that has satisfactory signal-to-noise ratio.

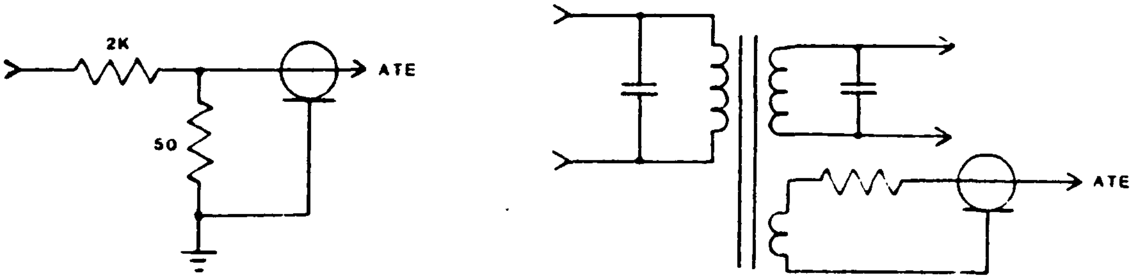


Figure 13-3. Techniques Used For Test Point Isolation

6. Adjustables and tunables should be minimized (see paragraph 12.1.5).

7. Modular, replaceable RF components should be used for all standard active circuit functions such as amplifiers, switches, mixers, etc. The design will be much easier to troubleshoot, and the specification and acquisition of components fro.n alternate/multiple sources during the production phase will be easier to control.

8. Active frequency multipliers should be avoided and division schemes or phase lock techniques used whenever possible. Adjusting the required nominal/tunable circuits is time consuming, and consistent sets of RF transistors are difficult to obtain.

9. Pre-aligned frequency selective networks are strongly suggested thereby avoiding the need for time-consuming manual alignment at the ATE station.

10. A means for opening automatic gain control (AGC), automatic frequency control (AFC), and other feedback loops should be provided or an appropriate summing junction which will allow the measurement of open loop parameters under closed loop conditions.

11. An RF or IF path with a frequency conversion is very difficult to test under swept frequency conditions. The filter characteristic in the module shown in figure 13-4 cannot be displayed on a network analyzer without a complex, external, frequency converting test fixture. This problem could be corrected by utilization of a test point.

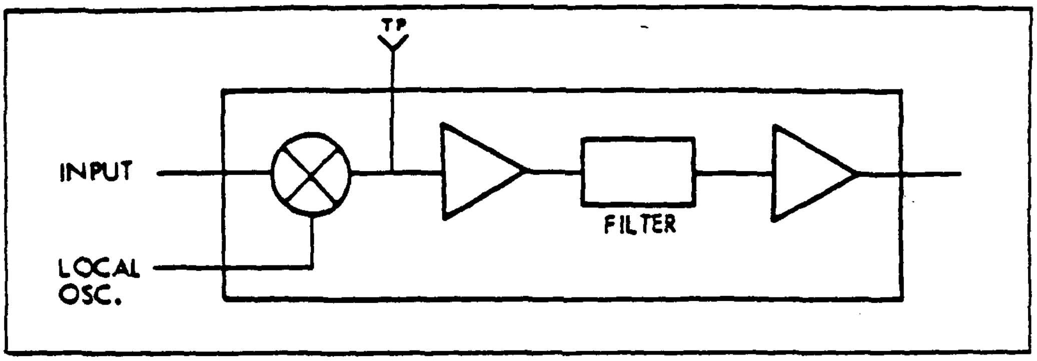


Figure 13-4. Addition of Test Point Following Frequency Conversion

12. Care should be taken to specify gain measurements such that the measured levels are sufficiently above the noise floor and sufficiently below the upper limit so that these effects do not influence the accuracy of the measurement. Waveforms and frequencies should be described at all interface points, and the limiting range and tolerances should be accurately specified.

13. Avoid designs that require tight absolute gains or phase shifts from components or printed circuit boards. Sufficient adjustment at subsystem(s) level can be built-in to compensate. If gain/phase matching is necessary, partitioning as shown in figure 13-5 should be attempted so that parallel channels are specified to track together rather than being of an absolute gain/phase.

14. Comparator and Sample/Hold Circuits are highly susceptible to noise and often fail test on ATE because of noise being injected from the test system. Filtering or buffers on the circuit board or on the test fixture can help. Partitioning the comparator from the RF detector in precision level detector circuits and making the detector output, comparator input and reference pins accessible to the ATE are suggested solutions.

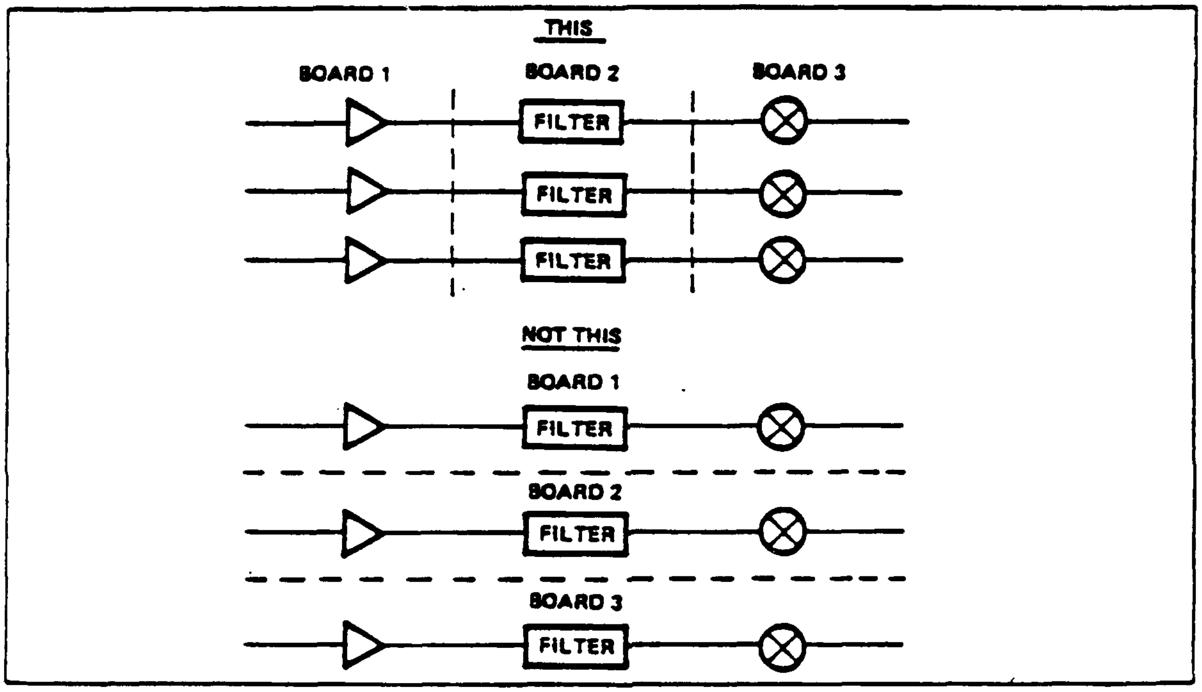


Figure 13-5. Partitioning of Matched Components

13.1.2 Specification Guidelines for High Frequency Circuits. The following measurements are difficult to achieve on ATE and may possibly be avoided by the use of a sample test or design test philosophy at the CCA level. If 100-percent test is necessary, it should be done at as high a hardware level as possible. Use of design approaches that exceed specification requirements by a wide margin (if this can be achieved with reasonably priced components) is another possible method. Margins can also be widened by reallocation of system budgets and tolerances, if possible.

- AM/FM noise
- Noise figure
- Gain and phase tracking/matching
- Gain and phase linearity/ripple
- Gain compression
- IM distortion
- Absolute power within 0.2 dB
- RF detector linearity (RF level to DC)
- Voltage Standing Wave Ratios (VSWR) < 1.05
- Gain/attenuation > 60 dB or < -70 dB
- Wideband gain versus frequency (multi-octave)
- Measurements on pulse envelopes

13.2 Microwave Testability Guidelines.

The microwave spectral region is considered to be that portion of the electromagnetic spectrum where both distributed and lumped parameters are utilized and includes the frequency range from 300 MHz to 40 GHz.

Manv of the suggestions and standards presented throughout this manual are applicable to the microwave discipline. Above 18 GHz, automated network analysis equipment is not readily available without frequency conversion and its associated errors. It is particularly important that the designer identify at the beginning of the program the types of measurements and the equipment that will be needed at various points in the life cycle. Testability requirements and specifications should be defined and understood down to the lowest equipment levels, and adequate tradeoffs performed.

The principles of controllability and visibility at microwave frequencies are as important as they are at the lower frequencies, as are test point isolation and the use of standard connectors with consistent pin utilization.

Design for testability at microwave frequencies is an integral part of the design process, requiring active participation from the manufacturing facility and initiation at the beginning of the program.

13.2.1 Working Standards. Special test fixtures are frequently required during the testing of microwave components. Often these test fixtures are certified as being acceptable for use when a reference component or working standard is measured successfully. The risk inherent in the use of the reference is that during a production run its characteristics may change, or it may be damaged or lost. The ability to reproduce the working standard should be based upon National Bureau of Standards traceable measurement methods. An example is the use of a coaxial cable as a working electrical reference length for the fabrication of cables. The absolute electrical reference length should be specified in a document, which will permit the fabrication and measurement of a new reference cable utilizing a fundamental parameter such as group delay.

13.2.2 Component Tolerances. Brassboard testing and hardware validation should be verified with as many critical devices (diodes, transistors, field effect transistors (FETs), MICs, stripline, etc.) as is practical from more than one vendor. Circuit performance must not be dependent on unspecified component parameters. Short cuts here will cause difficulty during production when components from second sources or from different production lots are encountered.

13.2.3 Test Error Analysis. In addition to the brassboard testing, an error analysis must be performed on microwave assemblies to ensure that normal component tolerances and distributed parameter variations will not produce unacceptable production test yields. If a potential yield problem is anticipated, special steps can be taken to minimize it by:

1. Pretesting and selecting components at a lower level to eliminate costly rework.

2. Providing trimming adjustments for deviant parameters.

3. Providing an external system level adjustment that compensates (software control is a possibility).

4. Possibly reallocating known errors and guardbanding to guarantee acceptable performance at higher levels of assembly and at temperature extremes. Noise figure, oscillator phase noise, and oscillator or amplifier output power flatness requirements have traditionally been specified in an overly optimistic fashion.

A thorough review of test requirements and procedures must be done to ensure that all functions are tested over frequency and temperature ranges. Production testing should include random vibration, thermal shock, and thermal cycling to detect workmanship faults. Additionai tests must be performed at the subassembly level to detect marginal circuit performance that could cause costly diagnostic testing at higher levels of assembly.

13.2.4 Diagnostic Test Capability. Production test of microwave assemblies is usually performed on a compu.er-controlled test station such as a network analyzer. It is not practical, and frequently impossible, to perform diagnostic fault isolation testing off-line on a manually operated test station. Therefore, it is essential that circuit partitioning, test interfaces, and test software include fault isolation capability that permits a lower skilled operator to isolate faults to a failed component. Features to be included consist of:

- DC test points to verify control signals.
- RF coupled test points to verify signal power levels.
- Modular test programs that can be single stepped.
- Stored fault test matrix tables to direct test sequencing.

13.2.5 Incremental Testing. Preliminary microwave testing of individual components or groups of components is often desirable during production. This testing can be accomplished by designing a special test fixture that will permit an insertion loss or phase measurement prior to the completing assembly level where troubleshooting will be more difficult.

13.2.6 Partitioning. Circuits should be functionally partitioned to minimize the need for special test stimulus and measurement equipment. Circuit partitioning must be a tradeoff between a few complex circuits and many simpler circuits. Complex analog devices are often very difficult to test. The use of complex circuits will result in lower manufacturing cost, more repeatable performance and minimum interconnects, which contribute to higher reliability. However, many simpler circuits will ease troubleshooting since each module may be tested separately. The modules are usually connected to one another with SMA connectors which, in themselves, are not always repeatable and may cause some major unwanted reflections. To minimize this problem, it is sometimes helpful to build and test the many simpler circuit modules during the design phase and later integrate these modules and eliminate the connectors.

When two or more circuits are to be connected with or without connectors, the input/output characteristics of the two circuits must be specified to avoid unwanted interaction. Normally this means minimizing the VSWR at each of the two ports that are to be connected. Time domain analysis has been found very useful in eliminating the connector reflections and helping to predict how the circuit will perform when integrated with other circuits. The circuit/unit positioning within an assembly must also permit easy removal without disturbing those circuits surrounding it.

13.2.7 Test Points. A test instrument will always disturb the circuit under test to some degree. Care must be taken to avoid using an instrument with a different impedance than the module will see when integrated with other circuits, particularly when measuring active circuits that have an isolator in the applicatioⁿ The isolator may have impedance levels that are significantly different than the broadband 50-ohm impedance levels presented by most microwave test instruments.

Permanent accessible test points should be included at circuit locations that may prove to be inaccessible when the unit is assembled into higher levels of equipment. These test points will minimize the need for constant assembly and disassembly of the unit to verify correct performance, which can be particularly critical when the subunit contains state-of-the-art, high failure rate and/or fragile devices whosᴗ proper operation is constantly suspect.

An example would be a calibrated test point at the output of a solid state transmitter (with state-of-the-art Impatt diodes) connected tᴗ a rotary joint. This configuration would allow transmitter performance to be verified through the test point at the seeker level. Without the test point, frequent connection and disconnection of the cable between the two units would waste test time and eventually compromise the cable.

Test point access must be provided to closed loop parameters and critical control signals where multiple subassemblies are part of a functional test. The ability to open feedback loops is important.

13.2.8 Transmitter Sense Points. Transmitters should have adequate sense points to detect arcing and monitor stress levels on such components as high-voltage capacitors, pulse-forming networks, transformers, and high-power, high-cost amplifier devices. These points can be used for system readiness assessment, diagnostics and for system shutdown.

13.2.9 Dummy Loads. Adequately cooled dummy loads should be provided to allow maintenance without system radiation. Personnel must not be exposed to dangerous radiation levels during the test cycle.

13.2.10 Circuit Adjustments. Complex adjustments that will have to be redone when the hardware is integrated should be avoided at the lower levels of hardware. The complete adjustment should be accomplished at a higher level and, if feasible, only the range of adjustment verified at the lower level.

Use adjustable phase trimmers whenever possible to minimize handling, damage, and errors when phase adjustments are required.

13.2.11 Control Signals for Test Consoles and Target Simulators. Provisions for convenient access to critical signals in the unit under test through test connectors should be included to simplify the design of test consoles and/or target simulators.

13.2.12 Signal Injection Points. Signal injection points should be chosen that do not require high-cost signal generators (high power at high frequency).

13.2.13 Cables. The design and test of RF cables is one of the most frequently overlooked activities during the development phase. The following is a list of RF cable design guidelines:

- The bend radii on semi-rigid cables is critical and must be per design standards to avoid overstressing solder connections.

- Semi-rigid cables also must include mechanical stress relief to function over the specified environmental extremes.

- Avoid the use of different connectors which are similar in appearance so that connector damage due to mistaken identity during subassembly test is minimized.

- Use connector savers for fragile test connections.

- Adequate space to properly torque connectors is necessary.

- Critical cables should be burned in to reduce infant mortality failures and/or time dependent drift in performance.

- Cable test at both cable assemble and following subsystem installation should be planned to check for manufacturing defects such as broken wires, shorts, and assembly errors/damage.

NOTE: In addition, clamping devices to fasten cables in established routing patterns should be carefully selected to prevent physical deformation during assembly.

13.2.14 Testability Standards. The following should be observed in the design of microwave equipment:

- Identify critical devices and validate brassboard performances over the specified environment with several different units.

- Perform an error analysis to ensure that normal component tolerances and distributed parameter variation will not produce un?^^ceptable production test yields.

13.3 MMIC Testability Guidelines.

MMIC (monolithic microwave integrated circuits) comprise an emerging technology with applications in ground, air, and space-based RADAR. A major testability concern of MMIC assemblies is the mechanical layout and construction. At present mechanical design is driven primarily by electrical performance, system geometry (array element spacing), and cooling requirements.

13.3.1 Subassembly and Chip Test. Subassembly level may include single or multiple MMIC chips mounted on a thin film network (TFN). A subassembly may or may not include a carrier network. In order to interface the subassembly to the test system, a custom-designed fixture or RF probing device is used. In either case the RF and DC stimulus must be injected into the MMIC network via RF launches or needle probes. In order for either scheme to yield repeatable results at microwave frequencies, mechanical and electrical layout rules must be followed during the design phase of the MMIC.

13.3.2 References. Listed below are general rules and guidelines for testing MMIC subassemblies and chips using RF probes and test fixtures. Guidelines for using RF probes were taken in part from the following references. If RF probing is planned, the design engineer is encouraged to send for a copy of these application notes for a complete set of design rules.

1. "Layout Rules for GHz-Probing," Cascade Microtech, Inc., P.O. Box 1589. Beaverton, OR 97075-1589. (503) 626-8245.

2. Williams, Dylan F.; and Miers, Tom H.; "A Coplanar Probe to Microstrip Transition;" IEEE Transactions on Microwave Theory and Techniques; Vol 37, No. 7, July 1988, pp 1219-1223.

3. Fraser, A.; Gleason, Reed; Strid, Eric; "GHz On-Silicon-Wafer Probing Calibration Methods;", 1988 Proceedings of the 1988 Bipolar Circuits and Technology Meeting; pp 154-157.

4. P.J. van Wijnen, et al.; "A New Straightfoward Calibration and Correction Procedure for On Wafer High Frequency S-Parameter Measurements (45 MHz-18 GHz);" Proceedings of the Bipolar Circuits and Technology Meeting; 1987.

13.3.3 DC Stimulus. The DC stimulus to the MMIC network is typically provided through one of the following three methods: (1) bias tee, where the DC is coupled through the RF path; (2) single needle probes or 'pogo' pins (fixtures); or, (3) multi-contact probes. Needle probes typically have their own manipulators for accurate alignment on the MMIC DC pad. Multi-contact probes provide all stimulus and grounds through multiple contacts on a single probe head. In high volume production a more practical solution is to provide all the required stimulus by using a probe card or multi-contact probes. In this case the following guidelines should be followed:

1. Mechanical Guidelines.

   a. Select pad footprint to meet requirements of selected probes.

   b. Pads should be located on outside perimeter on MMIC or TFN for easy access.

   c. Pads must be located on top side of MMIC or TFN.

   d. Pads to be contacted by a multi-contact probe head should be collinear.

   e. Minimum pad size to be used is 50 x 50 μm, although in general 100 x 100 μm is recommended.

   f. The minimum center-to-center pad pitch is 50 mm, although 150 mm is recommended.

   g. When using fixtures, pad locations should be standardized wherever possible to reduce inventory of required test fixtures.

2. Electrical Guidelines.

   a. At least one ground pad must be available for each probe. Alternatively, returns may be routed through the carrier plate with via grounds on MMICs and TFNs.

   b. All stimulus grounds must be electrically connected on the MMIC.

   c. Care must be taken to minimize current at each contact. Currents should be limited to 0.5 amps per contact maximum. This can be realized by using multiple contacts per function if the current exceeds this limit. Minimizing current will prolong the life of the probe contacts.

13.3.4 RF Stimulus (Using Test Fixtures). In a fixture, the RF stimulus is provided via a launch or bond wire to the TFN. The fixture will then typically provide a coaxial connector interface to the test equipment. Due to the relatively small sizes associated with MMICs the following guidelines should be followed.

1. Mechanical Guidelines. RF input and output should be located on opposite sides of the TFN. At a minimum, RF input and output should be located orthogonally.

2. Electrical Guidelines.

   a. Losses for input and output fixture halves must be well-characterized electrically, so that their effects can be de-embedded from the measurement data file.

b. Substrates with TRL (Thru - Reflect - Line) standards may be designed to perform calibrations directly at the fixture/Device Under Test (DUT) interface to eliminate the need to de-embed the measurement data file. These standards must be designed in for the same fixture as the DUT.

13.3.5 Stimulus (Using RF Probes). When using RF probes to provide RF stimulus to the MMIC the same guidelines used for DC stimulus apply. Additionally the following guidelines apply.

1. Mechanical Guidelines.

   a. Select pad footprint to meet requirements of high frequency probe configuration to be used (e.g., signal-ground, ground-signal-ground, signal-signal).

   b. Pad pitch should be designed to meet available RF probe pitch requirements.

   c. Maximum pad height variation in a row of pads contacted by a single probe (e.g., ground-signal-ground) is 0.5 mm.

   d. Verify maximum planar deviation of a row of pads contacted by a single probe is within the probe manufacturer's specifications. (Typically 5 parts per 1000.)

2. Electrical Guidelines.

   a. Orient high gain signal pads as far away from each other as possible. For example, input and output pads of an amplifier should be ideally placed on opposite sides of the MMIC. This layout will also minimize cross-talk problems due to capacitive or radiated coupling between probes.

   b. Provide a minimum of one ground pad for each high frequency probe.

   c. Refer to probe manufacturer's specifications and references listed above for additional application notes.

13.3.6 Circuit Adjustments. Avoid complex adjustments that will have to be performed again when the subassembly is integrated at the next higher assembly level. This minimizes the amount of test time required at subassembly level and eliminates needless adjustments. If possible only the adjustment range, or the ability to perform a gross adjustment, should be verified at this level of test.

13.3.7 Module Test. A module is typically made up of several MMIC subassemblies or chips mounted with TFNs on a common base. The chips/subassemblies are epoxied or soldered into the module housing and then interconnected using gold bond wires. Various other technologies other than GaAs may be used within the module. Typical circuitry includes silicon digital control circuits, silicon bipolar devices, and other microwave elements such as circulators, chip capacitors, resistors, etc. A common module configuration used in several early module development programs includes completε transmit/receive (T/R) functions in a single module. Some of the subassemblies that make up a T/R module include driver amplifier, pcwer amplifiers, phase shifters, and low noise amplifiers.

13.3.8 Test Fixturing. In order to interface the module to the test equipment, a test fixture must be used. The test fixture is required for several purposes. First the fixture prc vides an interface to the module RF, DC, and control functions. The fixture also serves as a mechanical support for the module. The fixture can be interfaced to thermal equipment to regulate or vary the module housing temperature during test. To support the high volume test requirements that will be associated with future module development programs, the fixture should be designed to minimize the time associated with having an operator load and unload the DUT.

:3.3.9 Connectors. As module sizes are reduced and multiple modules are mounted in a single housing, it is becoming increasingly difficult to provide standard coaxial connector interfaces on the module. This creates problems in performing network measurements ᵇecause the measurement reference planes cannot easily be defined with available calibration standards. For module connectors the following guidelines should be followed.

1. Wherever possible provide a standard connector interface at the module RF inputs/outputs.

2. If connectors cannot be used, access to a 50-ohm coplanar transmission line should be provided to facilitate fixturing or RF probing of RF inputs/outputs.

3. If connectors are mounted on the fixture, they should be a standard connector type for which calibration kits are readily available. (e.g., 2.4 mm, 3.5 mm, 7 mm, SMA, etc.)

4. Losses encountered in connectors not located on the module must be accounted for in the module test specification limits, or de-embedded as a post process after test.

13.3.10 Fault Isolation. During module RF test, the test operator must be able to trace failures to the subassembly/chip level if subassemblies were tested prior to being mounted into the module, a common module failure is missing, or damaged bond wires. These failures can be easily repaired if some basic layout guidelines are followed. Built-in test (BIT) techniques can also be designed into the module to help improve the fault isolation process.

1. Module fixture design should allow operator access to the top side of the module to accommodate use of a microscope and needle probes during functional test.

2. Wherever possible, subassemblies and TFNs should be mounted on a single plane. This will provide the operator access to all devices without disassembling the module.

3. Wherever possible, all bonds should be made on the top-side of the module. This will give the operator fault isolation capabilities while the module is still mounted in the test fixture.

4. Where space is available and when circuit performance will not be affected, additional test pads should be made available. This will aid in the troublechooting of malfunctioning subassemblies. Test points may include power supply monitoring, BIT signals, embedded control loops (e.g., gain control signals). Explore BIT methods that will allow some level of fault isolation from the module input/output. This is particularly important when testing and troubleshooting sealed modules.

5. To minimize the failures and test time at the module level, follow the guidelines below during design cycle and evaluation of the brassboard modules. The test specifications for the production units should reflect the results of these evaluations.

   a. Identify critical performance and validate brassboard performance over the specified temperature range with several different units. These results should be compared with predicted results using simulation techniques, if necessary.

   b. Perform an error analysis to ensure normal component tolerances and distributed parameter variation will not result in unacceptable production test yields.

   c. Reduce or add required production tests based on the results of testing brassboard and initial production units.

   d. When specifying test limits, consider tradeoffs: measurement accuracies vs system requirements and system test costs.

SECTION 14. HIGH POWER TESTABILITY GUIDELINES

14.0 OVERVIEW.

As with few other technologies, high power (typically line voltage and higher) designs can prove to be lethal to the user and especially to the test engineer if poorly designed, fabricated, integrated, and/or tested.

Designers of high power UUTs must be especially careful to provide protection to unit maintenance and test engineers since they often have to open and/or bypass initial protection barriers for troubleshooting.

There are two basic types of power supplies, regulated and unregulated power supplies. Avoid unregulated power supplies in modular designs, they cause too many headaches.

14.1 Regulated Power Supplies. There are two basic categories of regulated power supply designs; linears and switchers.

1. The Linear Power Supply (transformer, rectifier, filter, and voltage regulator). After the transformer steps down the line AC to a lower AC voltage, a full or halfwave rectification is performed and the resulting voltage is stored in a large capacitor. The voltage regulator takes the DC stored in the capacitor and the large riding AC component and smooths the voltage to a lower and regulated constant DC voltage. (See section 12.2.1.1).

   These supplies are generally used for low power levels, avoid using them for high power.

2. The Switcher Power Supply (see section 14.4.2) The switcher power supply eliminates the need for heavy transformer in the linear supply by directly rectifying the line voltage and storing this into a large capacitor (this capacitor now has a stored potential near the peak of the line voltage). Using a pulse-width modulator circuit or chip, the reservoir (capacitor) is pulsed at a high frequency (~20 KHz), rectified again, and filtered to a lower voltage.

   Recent advances in power ICs allow for line voltage to be directly tied to certain input pins of an IC while other pins provide +5V DC output directly to a circuit..

   Such ICs need to be clearly marked and protected with plastic shields to prevent a test engineer from hooking a DIP Clip to the device (with disastrous consequences) or mis-applying a scope probe.

Besides the basic differences of design for linear and switcher power supplies, higher voltage power supplies can be further broken down into two categories:

A. LINE FREQUENCY DESIGN

B HIGH FREQUENCY DESIGN

1. Line Frequency Design. In this case the capacitance across the load may be so large as to be a hazard not only to the power supply but also to all test and operating personnel. Typically for the 60 Hz line frequency 400 Joules (watt/sec) of stored energy is average. (4 to 6 Joules can be deadly).

2. High Frequency Design. The capacitance across the load for,these designs range between 1 and 2 Joules which usually is not fatal.

14.2 Corona and Electric Arcing. Corona , a visible phenomenon of an electric discharge, results from a partial electric breakdown. If a total electric breakdown occurs at a terminal of a HVPS, then a spark of high temperature ionized gas or electric arc may occur causing a short circuit. These sparks can be of enormous size and intensity for HVPS usually resulting in fires or personal injury. Corona can be accelerated by humidity, gas, vapors, and even dust near high voltage terminals. Corona left unchecked can produce ozone which reduces the normal air gap arc potential and attacks insulation causing it to become brittle and eventually fail.

Previous techniques used to control corona, encapsulated the high voltage sections in solid dielectric material or oil. Avoid these since they are difficult to access and messy to work with during test and maintenance. Several present day guidelines to control corona are as follows:

1. Use air encapsulation, providing low cost testing serviceability, reducing the weight of the supply. A disadvantage of air encapsulation is that a larger space is needed to house the power supply).

2. Check to see if a High Voltage and Field Gradient Analysis was performed on the high voltage design to ensure that correct utilization factors were used in generating the design.

3. Minimize high power interfaces.

4. Avoid awkward shapes and sizes for power supplies since mechanical packaging can impact the accessibility of the units. Failure mechanisms which are prevented by proper mechanical design include: insulation breakdown, thermal stress, and mechanical failures such as chaffing and cracking.

5. Avoid use of laminated insulating barriers and printed wiring boards. If unavoidable,provide shields/barriers. Make use of voltage gradient between capacitors per MIL-STD- 275 para. 5.1.4 (about 8 volts/Mil average).

14.3 Testability Guidelines for High Voltage/High Current Circuits. The most important testability rule for high voltage or high current circuit designs is to allow safe access by test personnel.

References should include company, state and/or federal regulations as applicable. Samples include:

- MIL-STD-454 reference 1.

- National Electrical Code - NFPA 70 and NFPA 70E-1979.

- OSHA 55 FR31984.

- NAVMAT P-4855-1A (NAVSO P-3641).

Design rules for testability include:

1. In areas containing test points, designers shall incorporate methods to protect personnel from accidental contact with voltages in excess of 30 Vrms or DC during normal operation. Proper labeling can be determined by referring to MIL-STD-454 (latest revision), Requirement 1, "Safety Design Criteria", Equipment Safety Markings.

2. When measurements excess of 300 volts are required, the equipment shall be provided with test points so that these voltages can be measured at a lower potential. In no case shall the measurement potential exceed 300 V peak relative to ground. This may be achieved by the use of voltage dividers of appropriate precision to drive test points for safety and accuracy. Test points above 30 Vrms shall be protected from accidental contact.

3. When using voltage dividers, the resistance path to ground must be made up of at least two parallel resistors of equal value for safety through redundancy. If one resistor goes open circuit, then the other resistor should be capable of maintaining the test point at a relatively low potential.

4. Minimize access to any hazardous circuit areas through the use of interlocked panels, barriers or enclosures (see table 14-1).

5. Use of voltage dividers is cited in MIL-STD-454, which is contractually invoked in nearly all Government programs.

Proper instructions in accident prevention and first aid procedures should be given all personnel engaged in high power electrical work, including design, fabrication, integration, and testing, to fully inform them of hazards involved.

Current rather than voltage is the most important variable in establishing the criterion for shock testing. Three factors that determine the severity of electrical shock are:

1. Quantity of current flowing through the body;

2. Path of current through the body;

3. Duration of time that the current flows through the body;

The voltage necessary to produce a harmful current is dependent upon the resistance of the body, contact conditions, and the path through the body(see table 14-2).

Table 14-1. Probable Effects of Shock

Current values (milliamperes)		
AC 60 Hz	DC	Effects
0-1	0-4	Perception
1-4	4-15	Surprise
4-21	15-80	Reflex action
21-40	80-160	Muscular inhibition
40-100	160-300	Respiratory block
Over 100	Over 300	Usually fatal

The resistance of a human body is typically from 1000 Ohms (wet skin) to 500,000 Ohms (dry skin). Sufficient current passing through any part of the body will cause severe burns and hemorrhages. However relatively small currents can be lethal if the path includes a vital part of the body, such as the heart or the lungs. Electrical burns are usually of two types, those produced by heat of the arc which occurs when the body touches a high-voltage circuit, and those caused by passage of electrical current through the skin and tissue.

There are various methods of incorporation of adequate safeguards for personnel, many of these methods being implicit in routine design procedures.

While current is the primary factor which determines shock severity, protection requirements are based upon the voltage involved to simplify their application. All voltages expressed in this standard apply to the DC value or the RMS value for AC. In cases where the maximum current which can flow from a point is less than the value shown above for reflex action protection, requirements may be relaxed with the approval of the procuring activity.

Table 14-2. Suitable Internal Protective Measures

Voltage range	Type of protection 2/								
	None 3/	Guards and barriers	Enclosures	Marking		Interlocks		Discharge devices	
				Caution	Danger	Bypassable	Non- 4/ bypassable	Automatic	Shorting Rods
0 - 30 Volts	X								
>30 - 70 Volts	X							X	
>70 - 500 Volts		X		X		X		X	X
>500 Volts			X		X		X	X	X

1/ Table is for reference only. (MIL-STD-454)

2/ Confine the application of headings to voltage ranges indicated. More than one option may be available on design requirements.

3/ Although no specific requirements exist for servicing 0-70 volts, designs should be reviewed for possible hazards in accordance with Table 14-1.

4/ Designs may use nonbypassable interlock applications below 500 volts, but the intent here is to imply complete enclosure.

14.3.1 Voltage Power Supply Mechanical Guidelines For Testability. Designing high power modules for testability and safety require certain mechanical guidelines as to vertical and horizontal working clearances for certain voltages (see tables 14-3 and 14-4).

Table 14-3. Working Clearances Horizontal Applications

Nominal Voltage To Ground (Peak)	Minimum Clear Distance For Condition (Ft)		
	#1	#2	#3
30 - 150	3	3	3
151 - 600	3	3 1/2	4
601 - 2500	3	4	5
2501 - 9000	4	5	6
9001 - 25000	5	6	9
25001 - 75KV	6	8	10
76KV - 100KV	8	10	12
101KV - 500KV	15	15	15
501KV - 1000KV	25	25	25
1001KV - 1500KV	35	35	35
1501KV - 2000KV	45	45	45

Table 14-4...Working Clearance Vertical Application

Elevation of Unguarded Energized Parts Above Working Space Floor

Voltage Between Phases or To Ground (Peak)	Minimum Elevation Above Working Space Floor (Ft)
50 - 600	8 Ft
600 - 7500	8 Ft, 6 In
7501 - 35000	9 Ft
Over 35KV	9 Ft + 0.37 In per KV above 35

- Power sources capable of supplying high currents can be hazardous, regardless of the voltage at which they operate because of arcing and heat generated if accidently short circuited. All power busses supplying 0.25 amperes or over shall be protected against accidental short circuiting by tools or removable conductive assemblies. This may be accomplished by one or more of the following methods:

  a. Use of guards and barriers.

  b. Sufficient space separation to prevent short circuits.

  c. Caution signs.

- All areas involving potential electrical exposure must be correctly and clearly marked with the appropriate hazard warnings for that situation.

- Locate circuit boards and other replaceable assemblies, fuses/circuit breakers, controls, test and adjustment points, etc., well to the front or, preferably, on a front panel that does not require entry into a high voltage/high current enclosure.

- Ground connections to shields, hinges and other mechanical parts shall not be used to complete electrical circuits.

- A point on the electrically conductive chassis or equipment frame shall serve as the common tie point for static ground and power ground. The path from the tie point to ground shall:

  a. Be continuous and permanent.

  b. Have ample carrying capacity to conduct safely and fault currents that may be imposed upon it.

  c. Have impedance sufficiently low to limit the potential above ground and to facilitate the operation of the over-current devices in the circuits. Unused wires installed in lines, conduits, or cables shall be grounded to prevent stray, static, or induced potentials.

  d. Have sufficient mechanical strength to minimize the possibility of ground disconnection.

- Connectors shall be selected and configured so that it is impossible to insert them in such a manner that subjects test personnel to hazardous conditions. Exposed pin contacts shall not be energized after being disconnected.

- Provision for shorting bars and rods is required if the circuit does not resistively discharge high voltages, 30 volts or more, within 2 seconds of power removal. In any case, shorting rods are mandatory in the case of exposures to = >500 Vrms or DC.

- If equipment voltages greater then 300 V peak must be measured, connections must be made and broken with the power off and the equipment properly discharged.

- Rigorously detailed operational or maintenance procedures are not acceptable substitutes of an inherently safe design. Circumstances precluding the use of guards, barriers, or interlocks must be documented. In any case, equipment design reviews must examine conformance to existing company and/or state requirements and/or MIL-STD-454.

14.4 High Power Testability Guidelines.

14.4.1 Testability Guidelines For Monitoring And Control Circuits. Testability guidelines for monitoring and control circuits are as follows:

1. Metering, display, or LED circuits are much easier to test if the display drive lines are accessible to the ATE system (see figure 14-1).

2. RF meters in drive-critical circuits should be placed as close as possible to the driver element for detection of feed line and VSWR problems.

3. Controls and indicators should be contained on an assembly separate from the one that contains the High Voltage electronic circuits. This permits fully automatic tests on ATE of the electronic parts, and manual test of switches and indicators with standard general purpose instruments (an ohm meter is usually sufficient).

4. Unless otherwise specified in the equipment specifications, meters shall have provision for overload bypass or alternate protection to eliminate high voltage potential or current at the terminals in the event of meter failure.

5. Control switches that are an integral part of an electronic assembly should have a test position that permits automatic remote control of the electronic circuits at the ATE station.

6. Any transducer electrical interface should be accessible to the ATE system and/or BITE. This covers such varied transducers as loud speakers, CRTs, and accelerometers and includes any conversion of electrical energy to or from the following energy forms:

   - Optical
   - Audible
   - Mechanical (position, speed, pressure, etc.)
   - Temperature
   - Magnetic

14.4.2 Switching Power Supplies For High Power. For high power circuits, always use a line powered switching power supply.

Many electronic modules using incoming AC lines employ "off-line-switcher" power supplies to rectify and filter the current to produce 250 to 300 VDC. The voltage is stepped down by electronically chopping it at the high frequency, employing wave rectification, and filtering to get a low voltage high current output needed for most modules.

Switching power supplies, as opposed to linears, make excellent high power supplies due to their high efficiency (keeping them cool) and low weight and size (due to absence of a low freq. transformer). Unfortunately, switchers are extremely noisy.

Also, switching power supplies need to be carefully designed so as not to induce too much harmonic distortion on AC power wiring. This can overload the neutral wire (especially 4 wire 3-phase power systems) to the point of causing fires.

The Department of Defense is releasing a specification for switchers over 300 watts to meet certain harmonic content limits. This should take effect in 1992.

A few additional recommendations for switcher power supplies are listed below.

1. Always use extreme caution when testing/debugging switchers since many of the components are at line potential. Do not clip your scope probe ground to these components.

2. Make sure that the rectifier is designed with an autonomous outboard SCR-type crowbar (to provide for over voltage shutdown).

3. Switchers occasionally fail by blowing their insides to bits. Therefore, provide adequate mechanical shielding around switchers for protection.

4. Make sure SWITCHERS contain over-voltage, over-current protection.

14.4.3 High Power Switching. Always design high current switching in such a way as to turn on and shut down in a "graceful" manner by limiting the "in-rush" current. This can be done by using a regulator and related circuitry, or a slow-resistance thermister in series with an input.

Always make the circuit turn off the power to high current circuit portions except when they are in operation.

14.4.4 Wall Plug-In Units (For Modules). Wall plug-in units come in 3 varieties:

1. Plain step-down transformer
2. Filtered but unregulated DC supplies
3. Completely regulated power supplies, (Linears and Switchers)

14.4.5 Batteries. These are usually not associated with high power but they have some tricky problems associated with them. There are two general types; re-chargeable (secondary), and non-rechargeable (primary).

- When designing lithium batteries into a module, provide adequate warnings and physical protection (clear plastic shield, etc) since they can explode.

- Specify battery current charging procedures or they may acquire a much shorter operation life and fail during system operation.

- Design easy access to these batteries for testability and maintainability.

14.4.6 Uninterruptible Power Supplies. Uninterruptible power supplies usually contain a battery powered DC to AC converter with a 115 V 60 Hz output and it can have power ratings of many kilowatts. They provide power to systems/modules which are used in critical functions which could provide harm to personnel or systems if not designed correctly. They provide back-up power anywhere from minutes to hours.

Uninterruptible power supplies can also supply power for testing of critical systems in remote locations.

14.4.7 Solar Cells. Solar cells can deliver up to 100 watts to a matched load. In the past year their efficiency has greatly increased. Design them in such a way so as to be able to isolate the individual faulty cell for trouble.

14.4.8 RF Power. In many RF designs HVPS are used to run klystron microwave tubes which provide the energy necessary to accelerate injected electron beams (such as for antenna/radar systems).

- Be sure to provide these klystrons with properly controlled and monitored high anode voltage.

- Provide adequate mechanical protection for operator in case a klystron malfunctions. These malfunctions or failures usually result in electric arcs around 16,000 volts at a couple hundred amps, destroying most items in their path.

- Provide computer interfacing with fiber optic cables to isolate, monitor, and control each klystron so that in case of failure that tube is destroyed but the rest of the system remains intact since the energy surge can't travel down the fiber optic.

14.4.9 Communications. When designing telephone line cables or other communication transmission lines always use transient suppressors to guard against lighting strikes (10 KV at 1000 Amps). These can take the form of spark-gap surge arresters used in high voltage power lines over 200 Kv or as more recently developed varistors.

- Never connect anything to telephone lines without checking area regulation codes.

- Use the recent development of packaging communications power supplies in Modular Replaceable Units (MRUs) which each contain their own control and monitoring circuits and are easily replaceable and can be replaced in UUTs with multiple units without a loss in power.

14.5 General High Power Module Testability Techniques.

1. Always use a 3-wire line chord with neutral connected to the module housing where AC line power is required.

2. Provide a "strain relief" in the form of a removable line chord connector where applicable.

3. For multiple power requirements in a module, provide separate keyed connectors to prevent accidental power interchange.

4. When line voltage is attached directly to a module through a transformer always use Teflon "heat shrink" on the exposed plastic shield over all high power circuitry, clearly labeled, with only small access holes for test probes.

5. Always use input line filters as well as transient protectors (or suppressors).

6. Always use a "slow blow" resetable fuse in the power line circuit to prevent transient from blowing fuse (transient suppressors will take care of them).

7. Make sure that all cables attached to a high power module are capable of handling the kind of power required, and are in good condition (no cracks in insulation, etc.).

8. Never build/design a UUT/module to run off of a power line without a transformer for isolation.

9. When possible apply a "bleeder" LED across the capacitor output to the discharge output capacitor in a few seconds under normal conditions. (Also it shows the test engineer that the capacitor is discharged - LED would need to be part of a lamp check circuitry to show that it has not failed).

10. All power supplies should be provided with over-voltage and over-current protection circuits which can be quickly adjusted and reset.

11. Provide power supplies tied in parallel with independent controls accessible to the ATE so that a faulty parallel supply can be isolated from the others.

12. Avoid power supplies that include circuitry to drive non-linear loads if this is not required by the specification. Linear loads are much easier to model then trying to emulate non-linear loads.

13. Provide the power supply or module with ATE access in the form of a "test" connector so that voltage and power can be easily tested, possibly relieving the use for a complex test adapter.

14. Provide adequate warning for hot surfaces in power supplies (60 degrees Fahrenheit or more) and adequate power supply cooling to dissipate heat generated by high power circuits.

15. Magnetic components such as inductors and transformer should be designed to have adequate access for the ATE and in some cases to be easily removable during certain power supply testing.

16, Externally powered equipment (line power) should be designed in such a way that no part of operator accessible outer UUT parts are at anything other than ground potential (excluding antenna and transmission line terminals).

17. Provide power supply controls (gain, test point signals, etc.) with access at an edge connector (or even a test connector) so that the ATE can more easily automate the testing with minimum operator intervention.

18. For multistage amplifiers, provide test points at every amplifier output stage (at a minimum) so a failing stage can be easily isolated.

19. Provide easy access to any high voltage reversal controls with ATE. These controls should also be provided with interlocks to prevent accidental power voltage reversals causing UUT damage.

20. Always design HVPS in such a way as to prevent improper assembly construction, and integration. Positioning of all components, connectors, and cabling should be guaranteed by design and verified throughout the assembly, test, and maintenance process.

21. If an HVPS is designed in such a manner so that the Corona Inception Voltage (CIV) of air is exceeded by the electrical field stress, a temporary insulation must be used during in-process testing (i.e., air, gas, or liquid).

22. Make sure that when performing high voltage module tests for things such as dielectric strength, and over-voltage that all resulting damage and reduction of system life is within specification. These tests are performed since dielectric breakdown and corona are the two prevalent failure modes in high voltage devices.

23. HVPS and circuitry create a great deal of heat which needs to be dissipated by adequate cooling. Provide interlocks to equipment such that power can not be turned on until adequate air/liquid flow is present.

24. Embedded thermo-couplers should not be used in a high voltage fixed area for monitoring internal temperatures.

25. If used, provide shields and/or bleeder resistors to prevent generation of high voltage by leakage current paths through thermo-couplers.

26. If the operator or test engineer safety is in questions, use remote and/or automated equipment and discontinue high voltage for short periods of time to allow for data collection.

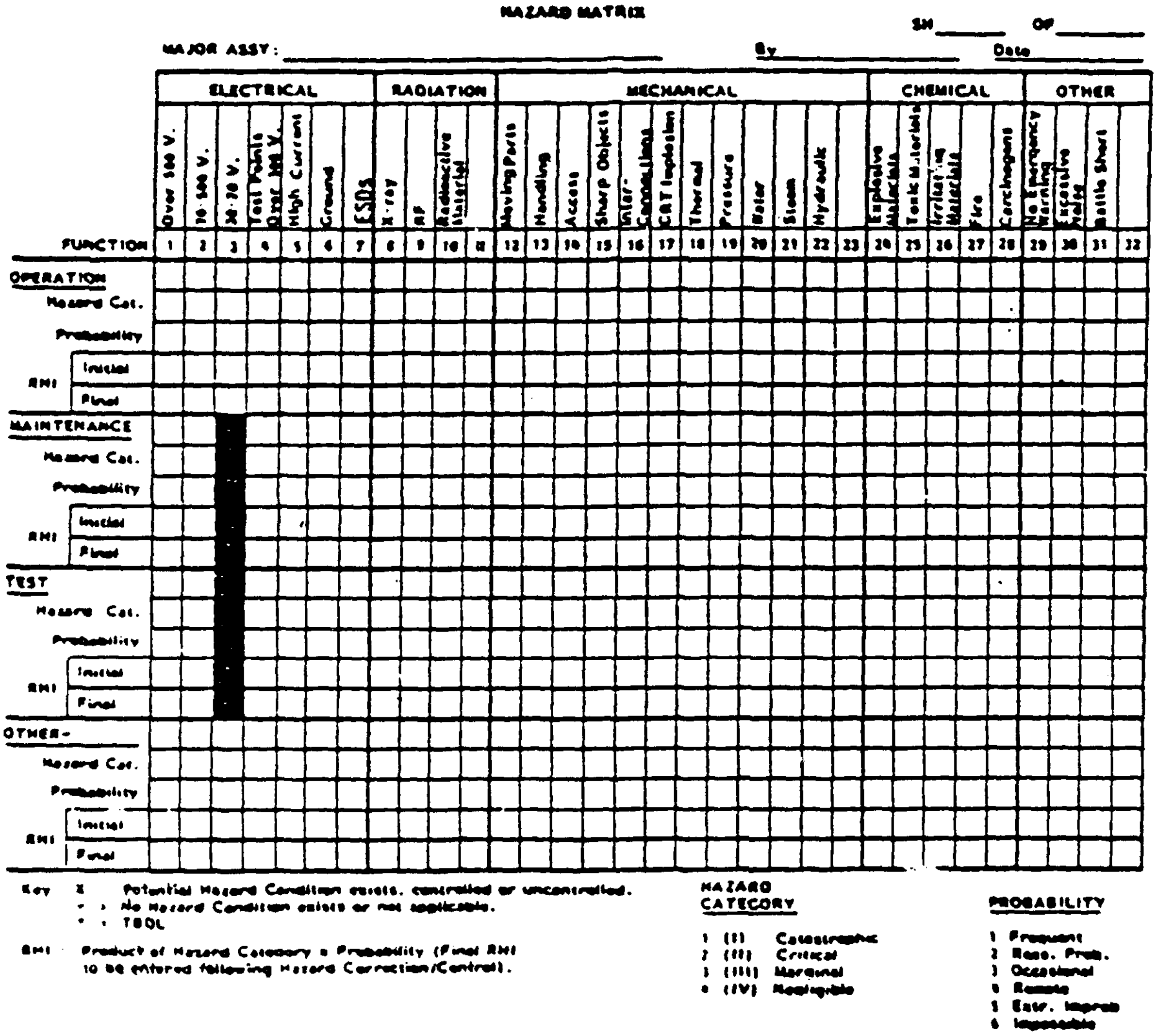
27. Design high voltage UUT to need a minimum of special tools for testing the unit.

28. Make sure high voltage UUTs meet all specifications for radiating EMI and/or X-RAYS for potential problems to ATE and personnel.

14.5.1 HV Environmental Testability Guidelines. High voltage systems will often require environmental testing such as "burn-in", high pressure, and altitude.

- When designing these high voltage units for environmental testability, specifications must be provided on the physical layout of the test area to guard against potential fires, explosions, and accidental high voltage contact by personnel.
- Provide adequate high power training requirements for operator, test and maintenance engineers.
- Control internal moisture condensation.
- Avoid pressurized high voltage units if possible.

14.5.2 Hazard Matrix. Create (or request) a hazard matrix for each completed major assembly, module, subassembly and/or unit where safety to the user and test engineers could exist (see figure 14-1).



HAZARD MATRIX

SH ______ OF ______

MAJOR ASSY: ______________ By ______________ Date ______________

	ELECTRICAL							RADIATION				MECHANICAL												CHEMICAL					OTHER			
	Over 500 V.	70-500 V.	30-70 V.	Test Points Over 300 V.	High Current	Ground	ESDS	X-ray	RF	Radioactive Material		Moving Parts	Handling	Access	Sharp Objects	Inter-Connections	CRT Implosion	Thermal	Pressure	Water	Steam	Hydraulic		Explosive Materials	Toxic Materials	Irritating Materials	Fire	Carcinogens	No Emergency Warning	Excessive Noise	Bottle Short	
FUNCTION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
OPERATION																																
Hazard Cat.																																
Probability																																
RHI Initial																																
RHI Final																																
MAINTENANCE																																
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Probability																																
RHI Initial																																
RHI Final																																
OTHER-																																
Hazard Cat.																																
Probability																																
RHI Initial																																
RHI Final																																

Key X Potential Hazard Condition exists, controlled or uncontrolled.
- = No Hazard Condition exists or not applicable.
* = TBDL

RHI - Product of Hazard Category x Probability (Final RHI to be entered following Hazard Correction/Control).

HAZARD CATEGORY

1 (I) Catastrophic
2 (II) Critical
3 (III) Marginal
4 (IV) Negligible

PROBABILITY

1 Frequent
2 Reas. Prob.
3 Occasional
4 Remote
5 Extr. Improb
6 Impossible

Figure 14-1. Hazard Matrix (sample)

14.5.2.1 Completing Hazard Matrix Forms. The first step in completing the Hazard Matrix for any unit shall consist of identifying the potential presence of each type of hazard; Enter an "x" or "-" as appropriate in the upper portion of the row/column block for operation, maintenance, and test functions. Note that an "x" indicates the hazard is potentially present, wether or not it is known that adequate safeguards have been, or are being, designed into the unit. A "-" indicates that the hazard condition does not exist, is too trivial to consider, or is not applicable. The row labeled "other" may be considered as appropriate: It is intended to be a miscellaneous row, providing a suitable place for any hazard entries not appropriate in the first three rows. Whenever an entry is made on the other row, a notation should be made to indicate the area of concern.

SECTION 15. INCIRCUIT TEST AND TESTABILITY

15.0 OVERVIEW.

Incircuit test (ICT) is a very popular technique used for both manufacture and repair. This section describes the basic philosophy and techniques used for ICT as well as provide design rules for testability.

15.1 Philosophy.

Incircuit Test (ICT) philosophy is based on the following assumptions:

1. If all components are of the correct value/function and they are correctly installed, the UUT is functional.

2. The majority of defects on a UUT are process induced.

Incircuit testers are very good at detecting and isolating manufacturing induced faults on a Printed Circuit Board (PCB). They test digital devices for truth table compliance and are able to make resistance, capacitance, and inductance measurements.

15.1.1 Techniques. ICT is founded on the simple concept of "isolate and conquer". Every component or interconnect on the UUT is verified independently from its neighbors and its circuit function. This depends on two basic requirements:

1. Electrical access to the components
2. Electrical isolation of the components

15.1.2 Access. Access in this instance means that the tester can make a direct electrical connection to every lead of a component under test. In other words, every circuit node on the UUT must be available to the tester. This access is normally provided by a special test fixture known, appropriately enough, as a bed-of-nails (see figure 15-1).

The nails on this fixture are small spring-loaded probes that contact the test pads or component leads on a UUT during test. The probes are mounted in sockets that are located on the fixture so as to line up with every individual node on the UUT. Connections to the tester are made by wiring the bottom of the sockets to interface cards or connectors that plug into the tester.

Most test fixtures are vacuum actuated. The UUT is placed component side up on the fixture and forms a vacuum seal with a diaphragm around the perimeter of the UUT. When the vacuum is actuated, atmospheric pressure pushes the UUT down evenly onto the spring-loaded probes. By this means, the tester now has direct access to every UUT circuit node.

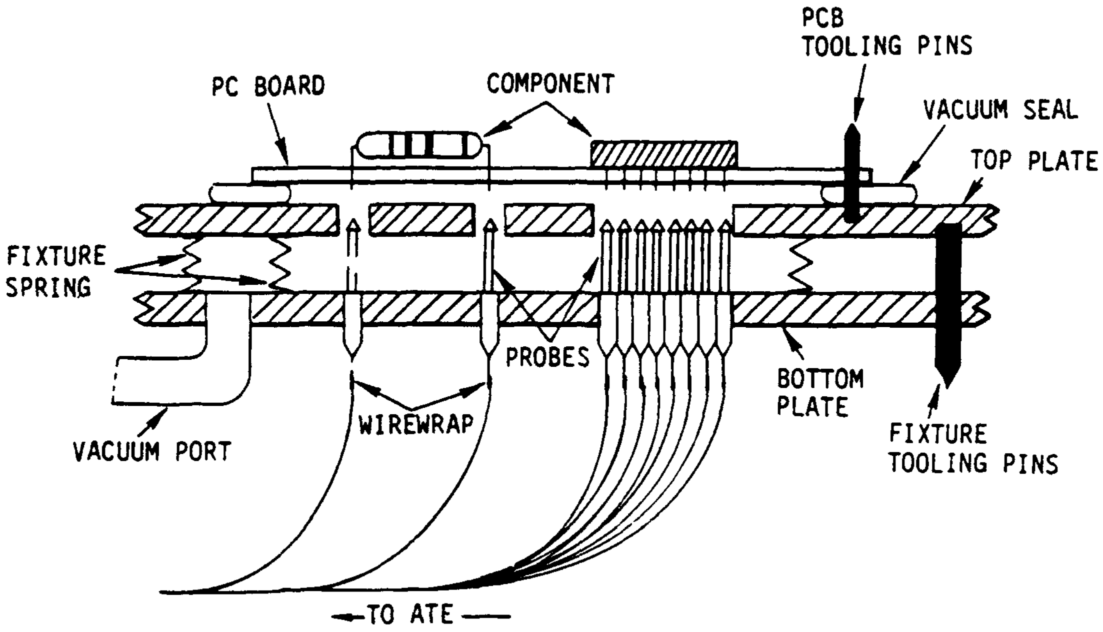


Figure 15-1. Bed-of-Nails Fixture

15.1.3 Isolation. Isolation techniques used by the tester differ depending on whether the device under test is analog or digital. Isolation of devices connected in a circuit is achieved by three basic methods: GUARDING for analog measurements and BACKDRIVING or DISABLING for digital device tests.

15.1.3.1 Guarding. Guarding is a method used to isolate passive/semiconductor devices when connected in a circuit. This method relies on Kirchoff's current law:

> "The sum of currents into and out of an electrical node equals zero."

The problem is to measure the current/voltage relationship of a device while it is being shunted by parallel impedance paths caused by t^h^e surrounding circuiuy. Guarding stops or significantly reduces the effect of these shunt paths while making the measurement. This is accomplished by:

1. Temporarily connecting all shunt paths around the device to ground (figure 15-2).

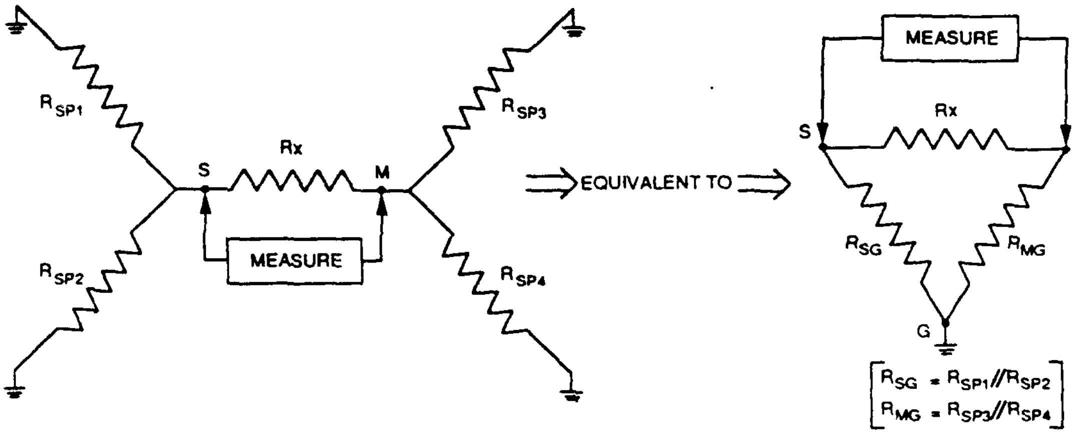


Figure 15-2. Guarding by Ground Shunt Paths

2. **Making use of an operational amplifier in the measurement circuit (figure 15-3).**

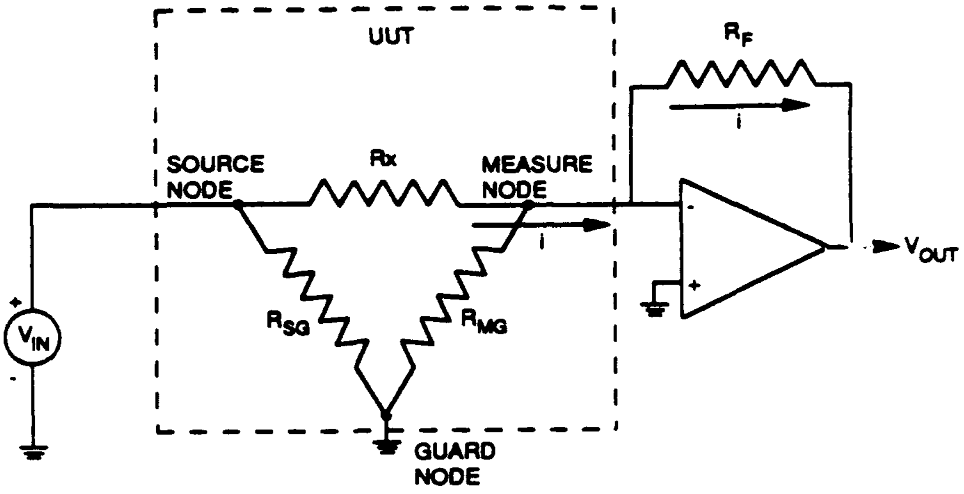


Figure 15-3. Incircuit Measurement Configuration

Figure 15-3 shows a typical measurement configuration that may be used in an incircuit test. The circuit takes advantage of the fact that the grounded positive input of the op-amp forces the negative input (summing junction) to remain at zero volts (this is known as a virtual ground).

As the measure node is a virtual ground and the guard node is also at ground, there is no current flow in Rmg. In effect, all the current (i) flowing through Rx will flow through Rf. Also, as the tester voltage source (Vin) and the feedback resistor (Rf) are known quantities and the output voltage (Vout) can be measured, calculating Rx is simple:

Vin/Rx = i = -Vout/RF

Rearranging terms gives:

Rx = - [Rf * (Vin/Vout)]

(The shunt path, Rsg, between the source node and the guard node has no effect as Vout depends solely on the current at the summing junction of the negative input.)

This technique disables the shunt paths and effectively isolates the device under test. The same technique can be used on any device where current and voltage are functionally related including capacitors, inductors, and semiconductors. Notice that no power need be applied to the board to perform these measurements. Typically, source voltages are kept low to avoid turning on any semiconductor junctions and source currents are also low, thus avoiding the possibility of damaging the UUT when a fault is present.

The source applied to the device under test (DUT) can be either voltage or current and either ac or DC. By this means, the technique can be tailored to measure resistive or reactive discrete as well as semiconductor junction voltages and transistor characteristics.

15.1.3.2 Back-driving. Back-driving or node-forcing is the method used on digital logic to test a target device as though it was disconnected from the surrounding circuit. The UUT is powered-up and the tester will drive the inputs of the device being tested through the necessary truth table and check for the expected output response.

If the logic states of the driving or upstream devices do not agree with those applied by the tester, the output of the driving or upstream devices must be forced to the correct levt. (figure 15-4).

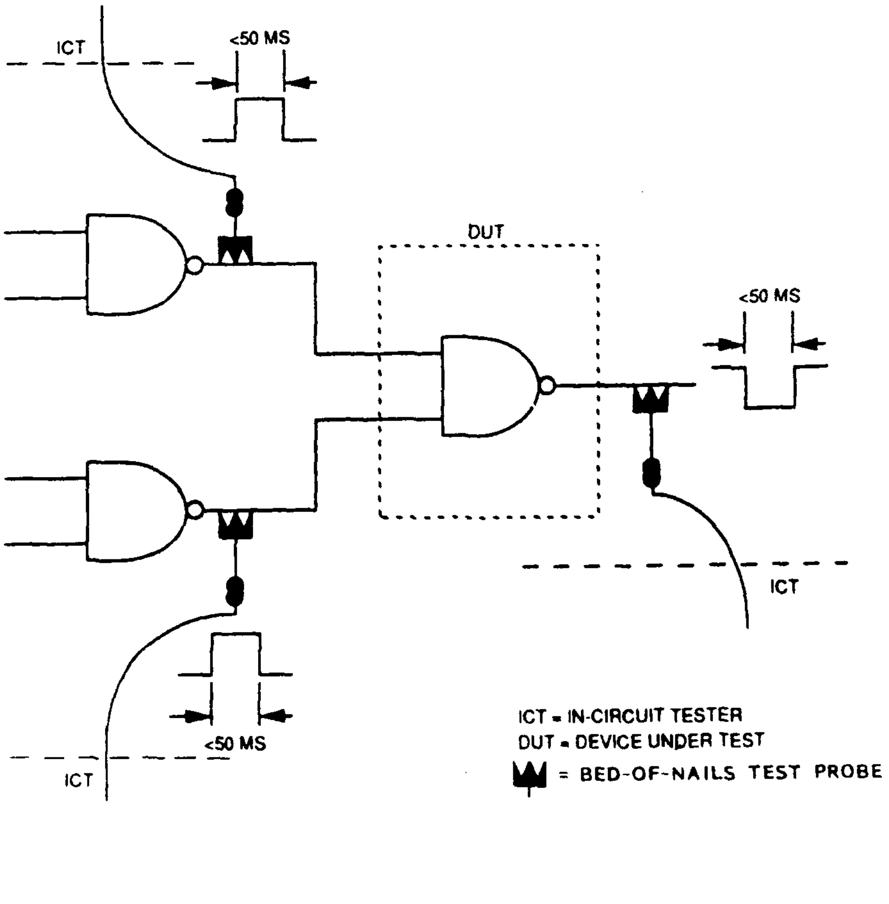


Figure 15-4. Backdriving

The amount of current involved in over-driving a device to the opposite logic state is usually in excess of the manufacturer's specifications. Superficially, this appears to have catastrophic consequences for the upstream devices due to the large amount of current involved in over-driving the device output junctions. Temperature rise caused by high currents could damage the output junctions or even melt the bond wires to the IC die.

In practice, if the temperature rise is limited by keeping the overdrive period short (usually less than 50 ms), no damage will result. Long term reliability studies using this technique have been performed and show negligible impact on the device life expectancy.

15.1.3.3 Disabling. The overall back-drive time to test a particular component is a function of the individual test vector time (typically 500 ns) multiplied by the number of test vectors (pattern depth). This means that SSI devices will not require long back-drive times because of the limited number of input possibilities.

Contrast this scenario to testing a memory, a microprocessor, or some other bussed device. Not only may the number of test vectors be large for a complex device, but a large number of nodes may need to be back-driven simultaneously.

For instance, a bus buffer may need to have all eight of its outputs back-driven to test a downstream complex device. If the ATE needs to back-drive 500 mA to control each pin, the device has to potentially handle 4 amps for the duration of the test. This will damage the buffer bond wires internally unless the number of test vectors is reduced. Fortunately, the Automatic Test Pattern Generator (ATPG) test generation process flags these problem areas and will not allow damaging tests to run.

Obviously, the proper approach is not to back-drive in this case but to disable the bus buffer. Assuming the bus buffer output enable pin is isolated from ground, the ATE can tri-state the outputs and thus pre-empt the need to back-drive.

Testability rules arising from this are:

1. Buffer large, complex devices with tri-stateable devices to enable using long test vector sequences. This is similar to the partitioning concept used in functional test strategies.

2. Provide individual device tri-state control whenever possible. (Although tri-state control lines may be shared between devices, make sure that disabling one device does not also disable the device under test!)

15.1.3.4 Isolation Techniques Summary.

Measurement Category	Isolation Method
Shorts/opens	N/A
Passive analog (resistance/capacitance/inductance)	Guarding
Un-powered active analog (diodes, transistors)	Guarding
Powered active analog (op-amps, comparators, regulators, etc.)	Not usually isolated
Digital logic	Back-driving, disabling

15.2 Advantages and Limitations of Incircuit Test.

15.2.1 Advantages (ICT vs Functional).

- Easy to program (80 to 100 hours for a typical 6 x 8 inch CCA)
- Compatible with automatic programming techniques (library based test generation)
- ICT test models simple to generate compared to functional test models
- Easy board handling (no cables or card extractors)
- Fast throughput (1-2 minutes for a typical 6 x 8 inch CCA)
- One pass diagnostics to component level
- Excellent coverage of process-induced faults (shorts, misoriented parts, wrong parts, etc.)
- Cheaper than simulation/guided probe functional test
- Incircuit ATE systems are generally cheaper than functional ATE
- Low operator skill requirements
- Sophisticated back-trace routines not required
- Automated fault/device data collection detects process problems or trends

15.2.2 Limitations (ICT vs Functional).

- Parametric faults may not be detected (e.g., parts interaction, timing, etc.)
- Limited truth table tests
- Limited test speeds and functional test capability
- Tolerance of tester vs tolerance of UUT (test fixture loading on every mode may cause measurement/performance limitations)
- Expensive fixturing
- Difficult to implement on new packaging technologies (SMT,TAB,etc.)
- Some components/circuits untestable
- Usually provides lower next assembly yields than functional test methods
- Difficult to test conformally coated boards.

15.3 ICT Program Generation.

As incircuit testing is oriented to testing individual devices, generation of ICT programs is a very straightforward task. The test parameters that need to be identified for each device are independent of its location and circuit function. This is due to the basic test philosophy of isolation. Typically, an incircuit tester requires a circuit description of the UUT with the following types of information:

Analog Components	Digital Components
Component type (resistor, capacitor, etc.)	Component type (74LS04, 54HC14, etc.)
Location (device lead X-Y coordinates)	Location (74LS04, 54HC14, etc.)
Identifier (R3, C88, Q21, etc.)	Identifier (IC3, U34, etc.)
Nodal connections (assigns node number or name to every device lead)	Nodal connections (IC3, U34, etc.)
Value (5 Kohms, 100 pF, etc.)	
Tolerance (+1%, +10%, etc.)	

This circuit description can be entered manually to a tester database or post processed from existing CAD/CAE databases. As the database follows much the same pattern for each device type, generally applicable device templates may be used. This makes possible the use of an automatic data entry post processor and an Automatic Test Pattern Generator (ATPG) (sometimes referred to as an Automated Test Program Generator).

15.3.1 Automatic Test Program Generator (ATPG). After manual or automated processing to provide an ICT compatible database, the target ATE uses an ATPG or A to create the test program and fixturing data (see figure 15-5).

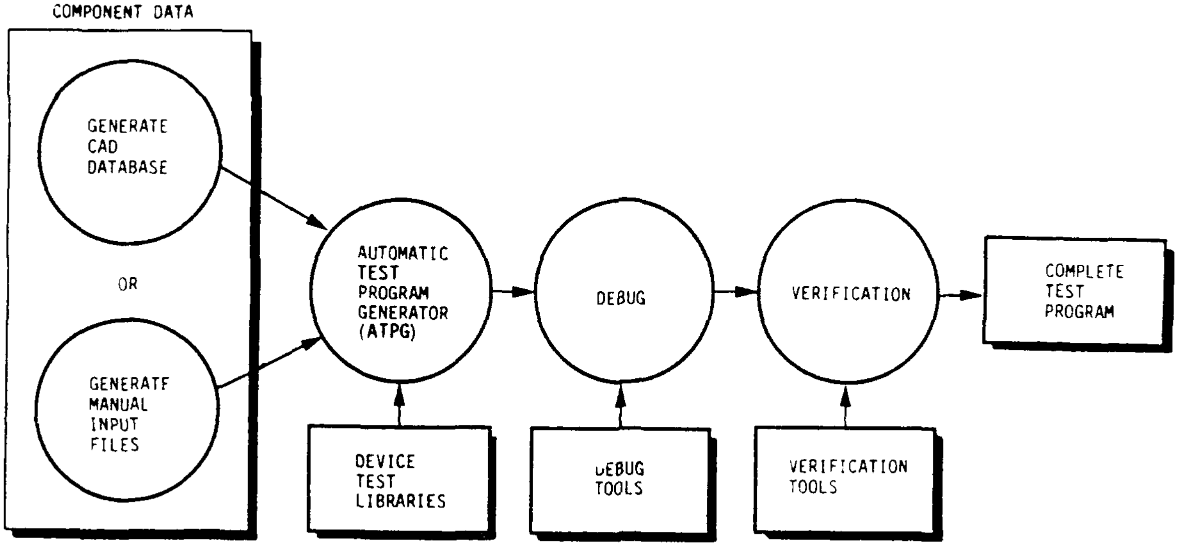


Figure 15-5. Automatic Test Program Generation

The ATPG handles the repetitive task of assigning device-specific data to general device test templates and typically generates the following:

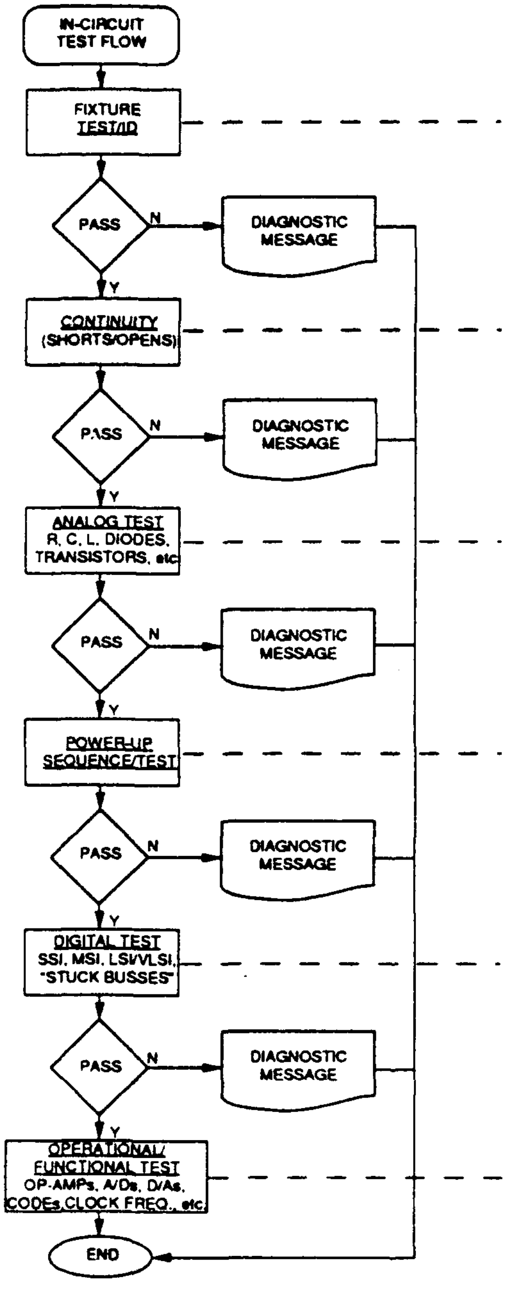
- Shorts/opens tests
- Analog discrete tests (UUT power-off)
- Digital device tests (UUT power-on)
- Fixture wiring details
- Test effectiveness analysis

While writing the analog test portion, the ATPG will analyze the circuit topology for guarding requirements to obtain the optimum test for each device. In doing so, the ATPG may take into account many potential sources of testing error, specifically tailoring the test conditions for each component. Specific corrections may be made for:

- Source impedance
- Tester connection impedances
- Settling delays
- Intrinsic measurement accuracies
- Tolerances of guarded devices
- System noise
- Non-ideal characteristics of the measurement operational amplifier

The ATPG will also write customized digital tests for the specific UUT topology, using templates from the tester digital test libraries. These templates or models are modified to resolve topology conflicts (e.g., tied DUT input pins) and to disable buses.

Finally, the ATPG assembles the individual tests into a coherent, executable test program (figure 15-6) ready for fixture debug and software integration.


IN-CIRCUIT TEST FLOW
FIXTURE TEST/ID
PASS
N
DIAGNOSTIC MESSAGE
Y
CONTINUITY (SHORTS/OPENS)
PASS
N
DIAGNOSTIC MESSAGE
Y
ANALOG TEST R, C, L, DIODES, TRANSISTORS, etc
PASS
N
DIAGNOSTIC MESSAGE
Y
POWER-UP SEQUENCE/TEST
PASS
N
DIAGNOSTIC MESSAGE
Y
DIGITAL TEST SSI, MSI, LSI/VLSI, "STUCK BUSSES"
PASS
N
DIAGNOSTIC MESSAGE
Y
OPERATIONAL/ FUNCTIONAL TEST OP-AMPs, A/Ds, D/As, CODEs,CLOCK FREQ., etc
END

Fixture test may use a shorting plate to check pin-bed. Can also check fixture mounted components and confirm the fixtue identity

Checks for shorts below a certain resistance threshold. Opens test is typically to confirm links and switches.

Unpowered test using small voltages/current to avoid UUT damage checks, actual values and tolerances.

Apply correct power sequence and check voltage/current

Powered-up library tests using backdriving/ guarding, as necessary.

Any powered-up analog or hybrid component/ circuits including functional tests or adjustments

Figure 15-6. ICT Test Program Flow (typical)

15.4 Testability Problems.

Testability problems with incircuit test are mainly caused by:

1. Mechanical designs that limit or prohibit access to the component under test.

2. Electrical designs that do not permit the component under test to be isolated from its neighboring components.

3. Devices on the UUT which are sophisticated and do not exist in the ATPG library.

15.5 Incircuit Testability Rules.

15.5.1 Mechanical Testability Rules.

1. Probe Access

   Probe access to all nodes must be available to the incircuit tester to enable individual device isolation and test. Usually all the nodes must be accessible from the solder side of the board for normal fixturing.

2. Board Perimeter Clearance

   Most incircuit testers use a vacuum actuated bed-of-nails fixture. A good vacuum seal between the UUT and the fixture is essential to bring the UUT in contact with the probes. To ensure this, a 0.25" minimum clearance must be available around the perimeter of the PCB, free of any components, pads, or hardware that interfere with the seal.

3. Via Holes

   All via holes must be filled to ensure a good vacuum seal with the UUT. Any leakage can prevent the fixture from actuating properly. If solder resist is used to cover via holes, the resist must make an adequate seal that does not break down under vacuum.

4. Component Mounting

   Do not design holes in the PCB to clear large component bodies or for any other reason. This increases the cost of the fixture due to the difficulty in making a good vacuum seal. Do not mount components on both sides of the board because this obstructs probing and causes fixturing problems.

5. Component Distribution

   Distribute test pads/components evenly across PCB. A concentration of probes in one area can cause uneven fixture actuation. The test programmer can usually select the probe locations to avoid this problem, but it can require a great deal of manual intervention with an automated fixture design program to achieve this.

6. Ceramic Boards

   Care must be taken when planning to test ceramic boards on an incircuit test bed. The force of a vacuum fixture can crack a ceramic board due to its stiffness.

7. PCB Warpage

   PCB warpage must be adequately controlled to avoid vacuum sealing problems. This includes specifying maximum warpage to the PCB manufacturer and designing board stiffeners to stop excessive flexing on large PCBs when the fixture vacuum is turned on.

8. Daughter Boards/Subassemblies

Do not mount daughter boards or subassemblies on the UUT. Unless complete nodal access is given to the subassembly components, the incircuit test becomes problematical. If a piggyback arrangement must be used, ensure that the subassembly is easily removable for separate testing. (Any subassembly for ICT should obey all the same testability rules.)

9. Board Size

Total PCB node count must be limited to 2700 maximum and board size limited to 10" X 12" maximum. Any larger than this causes problems with ICT program generation and fixturing. ICT ATEs are limited in the maximum node count that can be tested due to the factory hardware configuration or the ATE hardware architecture. Excessive node counts may require the factory to purchase and maintain extra ATE hardware or larger ATE systems. Both of these options are major expenses.

10. Lead Trimming

Ensure that device leads are trimmed correctly. Excessive lead lengths can cause mis-probing by the bed-of-nails or damage the probes themselves.

11. Tooling Holes

Incorporate at least two 0.125" diameter tooling holes per UUT, preferably three. These tooling holes must be registered to the PCB artwork and included on the PCB drill tape.

Tooling holes should be as far apart as possible and diametrically opposed. This gives good mechanical registration between the UUT and the bed-of-nails. (These holes are also used by automatic insertion/ placement machines.) Tooling holes must be un-plated and reserved only for fixture locating pins. Tooling holes must have a clearance area free of components and PCB traces (0.25" is an adequate clearance to the nearest component/trace).

12. Test Pads

If test pads are to be used, ensure that the test pad locations are included on the PCB drill tape and that the solder resist does not cover them. Use a 100 Mil grid array for test pad placement and a minimum clearance of 100 Mil to any component pin or via hole. Test pads should be solder covered to ensure reliable probing.

All test pads which will be probed by a "100 mil" probe must be at least 35 mils in diameter. Test pads must have a minimum 45 mils if they are to be probed by a smaller probe (<100 mil probe). Larger pads are required for smaller probe sizes because smaller probes have larger tolerances.

Test pads should be placed at least 200 mils from tall components (>200 mils tall) and 18 mils from anything else. This will ensure acceptable probe access.

13. Component Identification

Clearly label all parts, pins, and connectors.

Uniformly mount all devices in rows/columns using sequential numbering for device identification. This makes troubleshooting and repair much easier.

14. Obstructions

Any ECO wiring changes should be routed on the component side of the PCB. If the wires have to be run on the solder side, provide clear documentation to route the wires away from any component pads.

Do not cover any pads/leads that might be used for probe/diagnostic access. The PCB topology must allow access to every node. Conformal coating cannot be used on boards before test. Also, conformal coated boards cannot be retested on a bed-of-nails fixture because it is very difficult to reliably strip away or pierce the coating.

Do not mount components on the bottom of the PCB. If this is unavoidable, make sure that the component does not obstruct probe access or interfere with the vacuum seal.

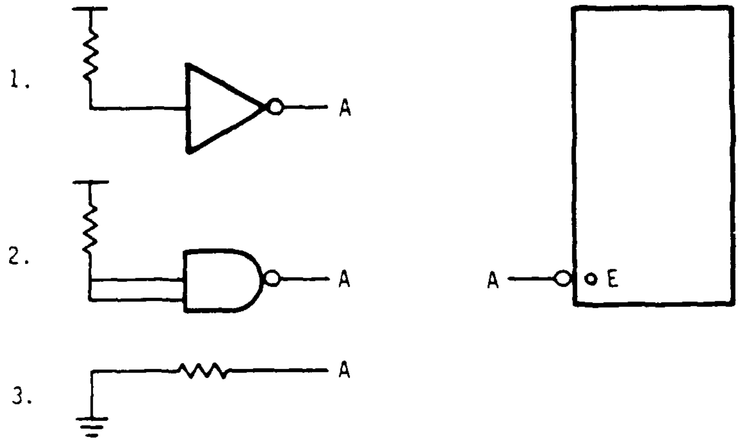
15. Repair

Large ICs (>24 pins) must be socketed for faster troubleshooting and repair. This also prevents potential PCB damage when unsoldering a large IC. Also, any programmable component is best socketed for easy upgrades. (These components usually have a higher failure rate in general than non-programmable components so easy repair is advisable.)

15.5.2 Electrical Testability Rules.

1. Tied Pins

Do not tie any device pins directly to VCC or ground. ICT test libraries assume that all device pins inputs are free to be driven high or low. It is always an opportunity to improve testability when a tied pin can be freed for tester access. A simple pull-up or pull-down resistor will provide the correct logic level to replace a rail. If noise is a consideration, a logic low level can be generated from a pull-up resistor and an inverter (see figure 15-7).



1/, 2/, or 3/ are all acceptable methods for the coupling enables from ground.

Figure 15-7. Controllable Tied Pins

2. Feedback Loops

Avoid feedback loops on individual components (see figure 15-8). Make sure any feedback loop contains a means for the tester to control the loop. If the loop cannot be controlled, asynchronous glitches are often produced during the test, causing spurious failures. Even if these glitches are not produced, a special test will be required to test that particular configuration of components in the feedback loop as a group. This means that the tester can no longer diagnose to the failing component, only to the loop group.

Not this

Combinational PAL fully configured.

PAL will decode select when testing memories. Unbreakable feedback loop will cause failures. Control feedback loop by adding gates to the chip select lines or by controlling the PAL directly (see figure 7-16).

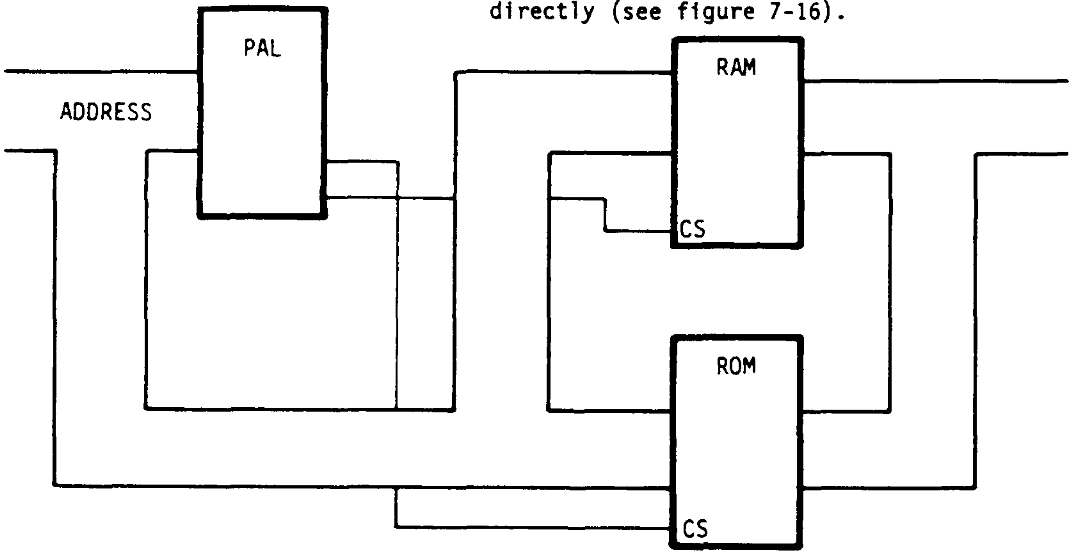


Figure 15-8. Feedback Loop

3. Control Lines

Provide individual pull-up/pull-down resistors on unused control lines. (reset/preset/tri-state, etc.). This enables excellent control of the UUT (see figure 15-9).

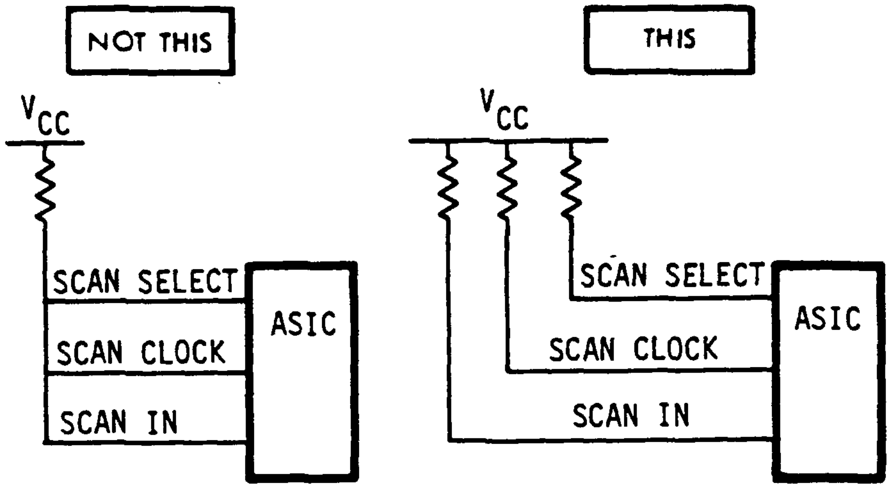


Figure 15-9. Controllable Control Lines

The ASIC scan control lines are tied together since the board function does not use the scan path. However, the incircuit tester needs independent control of these lines to apply the device test vectors correctly.

4. Noise

Provide adequate decoupling as close to each device as possible to avoid potential noise problems generated by the fixture.

Ensure ground and VCC traces are large enough to avoid noise problems

5. Analog/Digital Interfaces

Use a resistor or tri-stateable digital buffer to isolate analog circuits from digital circuits.

6. Fan-out

Never use maximum device fan-out capability. Remember that the ICT will act as one additional load.

7. Clocks/Oscillators

Always provide a method to disable on-board oscillators (see figure 15-10).

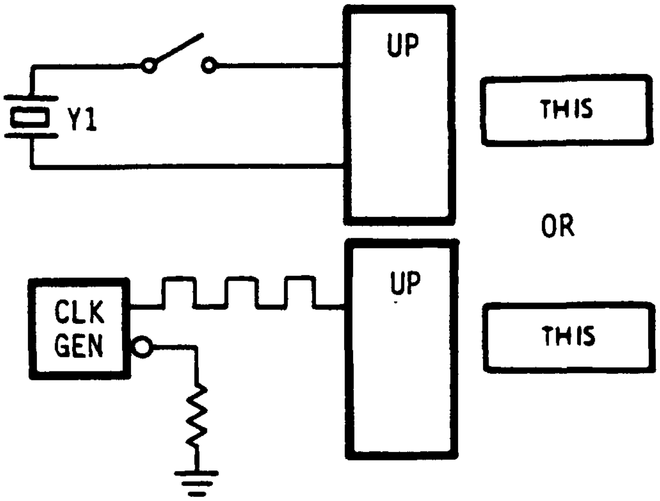


Figure 15-10. Controllable Clocks

8. Asynchronous Circuits

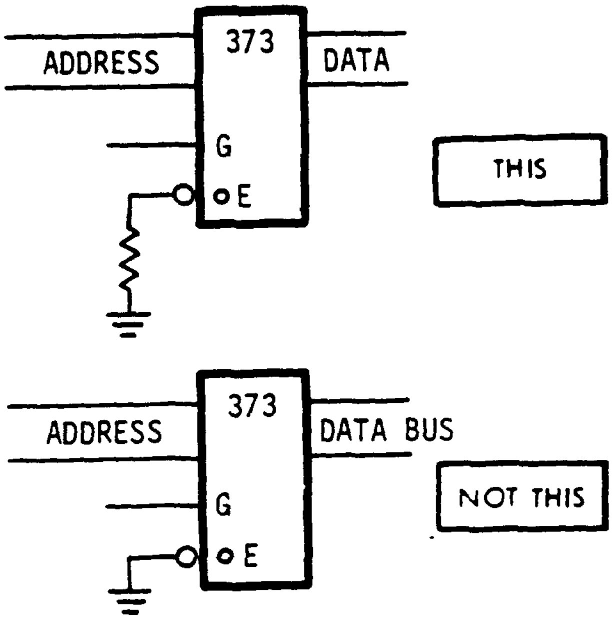
Avoid asynchronous timing circuits (e.g., one-shots, power-up resets). Asynchronous edges are difficult to control by back-driving and the resulting glitches may cause spurious failures. If these type of circuits are used, ensure that the ATE can disable/control them to avoid asynchronous activity.

9. Tri-stateable Devices

Provide a method to disable bus/tri-state devices. It is always preferable to disable device outputs rather than overdrive them. If possible, choose tri-stateable devices even if they are not required for the logic function and do not adversely affect the timing characteristics (see figure 15-11).

10. LSI/Microprocessor Based Designs

See sections 8 and 9 for designing with LSI/microprocessors. The guidelines in these sections also facilitate incircuit test. When choosing LSI/VLSI components, try to use components that have an existing ICT test for the target ATE.



Data lines can be tri-stated and do not need to be back-driven.

This latch may drive as many devices as fan out will permit. Back-driving the data bus lines simultaneously to test downstream devices is not advisable, especially if the back-drive time is high to test complex devices.

Figure 15-11. Control of Tri-states

11. Custom Devices

Provide easy LSI/memory initialization (less than 16 pulses on a single pin is desirable).

All PALs must be provided with easy initialization and direct tri-state control of the outputs. Most PALs oscillate when over-driven and, consequently, outputs must be tri-stateable.

If a PAL cannot be initialized then at the very least, the PAL outputs should be easily preconditioned to a high state. This usually will minimize the oscillation problem (see figure 15-12).

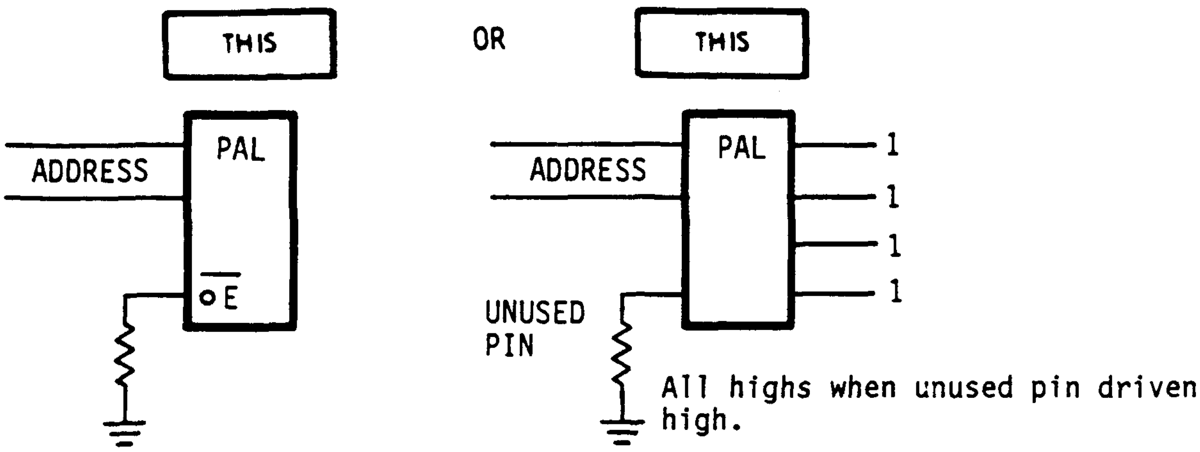


Figure 15-12. Preconditioning and Tri-stating PALs

All ASICs must be provided with easy initialization and direct tri-state control. Most ASICs are susceptible to damage when back-driving a large number of outputs simultaneously. This can have the effect of melting or weakening the ground supply bond wire(s) inside the device.

Provide test vectors for all custom devices (except ROM). Test length should not exceed 1000 vectors in any one burst/sequence to avoid excessive over-driving of surrounding circuitry. It is not necessary to provide a full functional test, only sufficient test vectors to check for process faults at the device I/O. This assumes that the device has been thoroughly tested to a high degree of confidence before assembly. Built-in device testability should be utilized (scan path, self-test, etc.).

Provide external access capability for single chip microcomputers. This enables the tester to take control of the microprocessor instruction sequence and to use an existing library test.

12. Wire OR/AND Circuits

Avoid wire OR/AND circuits. If these must be used, make sure the gates used are in the same IC.

13. ECL Outputs

All unused ECL outputs should be pulled down through a resistor on the module to prevent them from floating and possibly inducing noise. Some testers can automatically provide pull-up or pull-down resistors. However, if the unused ECL outputs are not terminated and a tester cannot provide automatic pull-downs then pull-downs need to be designed into the test fixture.

SECTION 16. ELECTRO-OPTIC TESTABILITY GUIDELINES

16.0 OVERVIEW.

This section has been added because Electro-Optics' (E-O) systems and modules are beginning to become more and more prevalent in today's military and commercial markets.

Lasers are used in thousands of differen. kinds of projects such as optical memory storage and retrieval, industrial cutting tools, medicine, communication equipment, range finding, alignment, reconnaissance, and just recently optical computers, to name a few.

Systems employing fiber optics are being used for communications and gyros in the military due to its inherent radiation hardened characteristics, light weight, and high tensile strength. Commercial use includes communication, medicine, and electronic systems.

Incorporating testability into the design of E-O systems and modules includes all of the suggestions made in the previous chapters and the following chapters wherever electronic circuitry is designed into the electro-optic module.

Electro-optic UUTs can be classified into two main types; active and passive.

1. Active E-O modules are defined as units which send out some form of radiation from a source through some media to a sensor/detector. This includes sending out radiation and receiving a reflection of it such as laser range finders, illuminators in weapons systems, chemical detection units, and wind shear instruments, etc.

2. Passive modules usually do not include a source and simply receive incoming radiation which is presented to a detector, the type depends on the wavelength of the incoming radiation. The detector could be a sensor or a detector chip. It could be cooled or not cooled. Examples include: radiometers, telescopes, microscopes, vision systems or even the human eye.

In paragraph 16.1 Electro-Optics definitions are introduced. Starting with paragraph 16.2 E-O is broken down into four major sections.

1. General E-O modules.
2. E-O Sources. (lasers, arcs,...).
3. E-O Components. (fiber-optics,...).
4. E-O Sensors/Detectors.

NOTE: The ensuing discussions are very general suggestions applying (in most cases) to all electro-optical frequency ranges from Infrared (IR) (2500 GHz) through the visible to Ultraviolet (UV) (10,000 THz).

Presently, there are so many different types of E-O components for which specific testability suggestions can be made that it goes beyond the scope of this handbook to include them all. Nonetheleꞩꞩ, the most commonly used components are presented in a reasonably comprehensive manner.

The following list shows the diversity of items in this field.

- Dozens of different types of lasers using solids, liquids, and gases including such exotics as copper or gold vapor, halogens, solvents, etc.

- ARCs pressurized to above 250 atmospheres.

- Optical lenses containing traces of radioactive thorium.

- Voltages to 20 KVs for lasers; currents above 100 amps for ARCs.

- Some of the most toxic gases known can be released by mishandling electro-optic UUTs , including chlorine, and various nerve gases.

- Lack of eye protection could easily lead to blindness on failure of optic devices used in some of these UUTs.

16.1 Definitions.

1. E-O system or LRU — A system made up of several electro-optic modules.

2. E-O Module/UUT — A separate laser, separate optics, or a detector or any combination thereof placed on a module or CCA. The lowest replaceable part of a system.

3. E-O adjustments and/or alignments — A form of testability in electro-optics.

4. Source(s) — Sources including all kinds of lasers: CW,pulse, solid, liquid, gaseous , IR, visible, UV; All types of ARCs, incandescent, Light Emitting Diodes (LEDs), etc.

5. Optical Components — Include mirrors, lenses, prisms, filters, quarter-wave plates,parabolas, photo-multipliers, etc. for IR, visible, and UV frequency ranges.

6. Fiber optics — Covers fibers used for image transmission and communications; single multi-strand, glass, plastic, etc.

7. Sensors/Detectors — Include photo-conductive, photo-voltaic, bolometers, thermopiles, pyro electric, CCDs, etc. for applications at room temperature or cooled.

16.2 General E-O Modules.

For the designer of E-O modules, not a new technology, (but presently a very rapidly expanding technology and picking up more momentum every year), the question should not only be "Will the UUT perform its desired function?", but also, "How testable is it for a given test personnel skill level?" A lower test technician skill level may require more training and/or more expensive semi-automated, totally automated test equipment,and/or support equipment.

During UUT design, cost tradeoffs need to be made to determine whether a subsection of a UUT should be a "throw away" unit or should be designed to be testable. "Throw away" units should be designed in such a way so that they are easily replaceable (without alignment or with minimum alignment). Present research is making this decision easier with several optic components on IC like chips to be placed in UUTs to do certain tasks and to be thrown out if not working correctly. Therefore the prime UUT designer should specify what needs to be tested by what skill level, with what equipment, and in what kind of an environment.

Building military optical equipment now (as of 1988) requires modular design and in most cases replacement of similar modules without realignment into the UUT.

Before E-O parts are built into a module, they need to go through some basic kinds of tests to see if they meet the design and manufacturing specifications for the specific module into which they will be incorporated. This prevents many hours of aligning a module only to find certain parts were defective to start with. These specifications and test results need to be available to the test engineer as a baseline.

For Infrared modules it becomes important for most applications to incorporate an active or passive form of thermalization to keep the UUT at a given temperature during operation and test.

Infrared modules using opaque lenses must be aligned using surface reflection techniques. If an image evaluation is required, a "knife edge" trace must be employed using an IR source and detector. IR design engineers must remind themselves that to design an IR module for testability, tests must be easy to be performed. Also, these modules may need to be tested in the field. This requires an internal reference like a small black body or an ice bath

Individually mounted optics can have up to 6 degrees (of freedom) of adjustment. Mounts with more than 2 degrees of freedom should be avoided since alignment becomes a nightmare.

16.2.1 General E-O Module/UUT Testability Guidelines.

1. Every section of design should be reviewed for UUT and personnel safety i.e., getting eyes, fingers into the beam with covers on or off; protection from high voltage and current, toxic gases and dyes, radioactivity, high temperatures, etc. and a Hazard Matrix filled out. See Section 14.5.2.

2. The source beam should be accessible and visible through easy-to-use cross hairs, and/or florescent blocks at every aperture or even superimposing a second visible beam on an otherwise invisible source beam.

3. With covers off, the UUT should operate fully, not somewhat or incorrectly (i.e., optical train should not be different with covers off).

4. All UUT/Component signals should be available with UUT turned on and covers on.

5. All E-O UUT data should be available (including schematics, parts lists, design concept memos, TRS, calibration and alignment specs., maintenance specs., optical criteria specs., and safety specs. regarding toxic gases, dyes, high voltage, high and low temperatures, high current, radioactivity, explosion hazards, etc.

6. UUT should be partitioned to physically separate source, optic train, sensor, and UUT electronics.

7. Avoid, if possible, the UUT's requirement of a clean room for aligning, debugging, or testing.

8. Design UUTs for easy spatial response measurement (i.e., use adjustable filters and /or interchangeable detectors.)

9. Avoid E-O UUT designs that are filled with a gas other than air (i.e., inert gases such as nitrogen, argon, etc.), unless the gas is an integral part of the design.

10. Design E-O UUT to be externally activated (stimulated) at least partially and/or supplied with simulated data where possible.

11. Design UUTs to have a temperature compensator for optics if applicable.

12. Design UUTs to have auto focus.

13. Design UUTs for course and fine external focus adjustments.

14. Design imaging UUTs so that the Modulation Transfer Function (MTF) can be easily measured.

15. Design the E-O UUT to have an internal reference or "built-in calibration".

16. For electrical-optical components, such as photo-multipliers, vidicons, CCDs, etc., design in easy access to all I/O and control lines.

17. Individual E-O modules should be electronically and physically accessible so that each can be individually tested.

16.2.1.1 E-O Testability Guidelines Based on Alignment.

1. Individual optical components, including sources and sensors, should be aligned elsewhere and installed in the module without module alignment.

2. Design E/O systems so that more than two degrees of freedom are not required.

3. E-O UUTs should be designed to facilitate automated alignment (i.e., using quadrant detectors, targets, receptacles, etc.).

4. Before aligning a UUT, all bonding agents on components should be allowed to cure and stabilize.

5. Avoid using films of adhesives for separating parts that need permanent alignment.

6. Avoid using "push-pull", "push-push", or set screws for permanently holding optical components.

7. E-O UUT alignment should proceed in a systematic fashion (meaning all optical and mechanical adjustments should be made in one pass through).

16.2.1.2 E-O Testability Guidelines Based on Adjustments.

1. E-O UUT adjustment hardware should be large and strong enough to support repeated adjustments with the amount of torque needed.

2. Adjustment mechanisms used should have sufficient "play" available to allow slow and smooth movements.

3. All "lock down" screws should be as insensitive as possible but easily accessible for adjustments even after the UUT has been assembled.

4. All adjustments involving metal flextures should be avoided.

5. Independent mechanical adjustments of E-O components should be possible with a minimum of backlash especially during "staking" even with the source on.

6. Individual components should be able to be operated without the entire module being on (i.e., source, sensor, etc.).

7. All special tools needed for adjustment should be documented and easily available.

16.3 Electro-Optic Sources.

There are many different types of sources used in E-O UUTs. Discussed herein will be: Lasers, Laser Diodes, ARCs, and Florescents (Incandescent Photonics)[1].

16.3.1 ARCs. High Intensity Discharge (HID) lamps are the most widely used for general illumination and in optical modules. There are many different types of ARCs including Compact Source ARCs, Capillary Mercury Lamp ARCs, Zirconium ARCs, Quartz ARCs, Spectral Lamp ARCs, etc. These sources can use less than 100 volts with currents as high as several hundred amps (see section 14 on High Power). They can be pressurized to 250 atmospheres and radiate energy in the infrared, visible and/or the ultra-violet range.

All ARCs are designed to operate most efficiently on alternating current requiring a ballast to give several hundred volts for ignition and stabilize operating current. When turned off, these lamps require several minutes for cool-down before re-ignition. If lamps are operated a few hours at a time each time they are turned on, lamp life time can exceed 10,000 hours. These lamps cannot be electrically dimmed without serious lamp life consequences.

16.3.1.1 ARC Testability Guidelines. When designing in an ARC SOURCE, make sure that operators and test personnel are protected by barriers from ARC failure, explosion, ARC radiation (if applicable), and excessive heat caused by long hours of ARC operation.

- Design interlocks to prevent ARC lamp access and removal when the ARC is still on and/or is not sufficiently cooled.
- Provide instructions near the area ARC access cover for ARC removal procedures.
- Design UUT for easy ARC lamp access and removal once the ARC has cooled. (cold ARC lamps can still explode!)
- For ARCs used internally to a UUT, provide a means of checking if the ARC is actually lit.
- Provide easy access to lamp ballasts.

16.3.2. Florescents, (Incandescents). These lamps are extremely common. They are used especially for incoherent illumination and should be designed into a larger module in such a way as to make them easily replaceable.

[1] Reference the PHOTONICS HANDBOOK, 1988, Book 2, 34th edition, put out by Photonics' Spectra magazine.

16.3.3 Light Amplification Stimulated Emission of Radiation (laser).

Lasers come in four flavors: Solid State, Gas, Liquid and Semiconductors which operate in the infrared, visible, ultraviolet and/or x-ray range either with pulses or Continuous Wave (CW). They are classified into four classes by the amount of power being radiated for continuous wave lasers (0.4 to 0.7 uM). (Reference ANSI Z136.1, latest version).

Class 1	≤ 0.4 uW.
Class 2	≤ 1.0 mW.
Class 3	≤ 0.5 Watts.
Class 4	> 0.5 Watts (for periods greater than 0.25 seconds).

Each class needs warning labels and operator protection as outlined in ANSI Z136.1 (latest version) and as may be outlined in state regulations (which can be different according to usage for every state in the US and in foreign countries).

Protection should be supplied to the operator and test engineers to block out most of the emitted laser radiation to achieve safe levels.

Working with lasers requires operators and test engineers to have been trained in the operation and care of E-O UUTs before operating, building and testing them. Lasers, besides emitting radiation that can harm an operator's unprotected eyes, also are operated at a potentially dangerous high power anywhere from several hundred volts to several thousand volts (see section 14 on High Power). Lasers' mirrors should always be at ground potential.

Lasers can come in many different packaging designs from bare tubes with bare electrodes and external power supplies, and totally enclosed units which need only be plugged into a wall outlet, to larger high power units which require large external power supplies.

Lasers (especially high power designs) tend to run hot and often need forced cooling either air or liquid.

- If at all possible choose air over liquid cooling for easier overall testability. Liquid cooling has many parts, (such as a pump, a liquid reservoir, flowmeters, and tubes) that are additional items that require testability to be designed into them and they often are very awkward to work around during UUT testing.

- Also caution should be used when working with laser gas mixtures which require periodic refilling (such as CO_2 and Eximer lasers). Besides the danger of inhaling these mixtures, there also exists the danger due to the high pressure involved during the filling process.

- Again, caution should be exercised by giving engineers adequate training and knowledge of the materials being worked with, provide adequate ventilation, and never allow an operator or test engineer to work long periods of time alone.

The basic 4 key parameters that must be easily testable for almost any laser include:

1. Output power — For a specific operating current, the output power must meet spec. to adequately operate the UUT.

2. Beam Diameter — Be able to use Ronchi Ruling method; also, check beam mode.

3. Beam Position — Determine the beam alignment relative to Laser mounting surface.

4. Heater Voltage (if applicable) — Measure heater voltage after a given number of seconds after turning power on to verify stable in-spec. voltage values.

Ideally, these tests or processes should be monitored automatically using Built-in Test.

- Wherever possible use current limited power supplies as a fail-safe mechanism for such "constant power" lasers such as the Argon laser.

16.3.4 Laser Diodes. With the advent of fiber-optics, laser diodes have become more and more important in the field of E-Os because of their small size and long lifetime (50 years with proper handling). They are available in a wide range of output power (both pulsed and continuous wave wavelengths (750 nm to 30 µM), and packages. They provide a coherent source of light as opposed to the defuse Light Emitting Diodes (LEDs). However, their sensitivity to temperature changes requires a controlled environment. Presently, laser Diodes come in two large classes: Gain Guided and Index Guided devices.

- Gain Guided devices have no refractive index profile built in the horizontal direction.

- Index Guided devices include a built-in refractive index profile in the horizontal direction. This keeps the propagating light wave parallel to the junction.

- Remember that CW laser Diodes can be operated in both continuous wave or pulsed mode (allowing for modulation up to 10 GHz). But that pulsed mode devices cannot be run in a CW mode without over heating and eventual failure of the device.

- Laser Diodes are very static sensitive and operator needs to be well grounded. They also have a shorter life than LEDs.

- Soldering iron tips should be grounded.

- Individual diodes should be shipped with their leads shorted together. Current transients and/or device overheating may result in device damage. Therefore, provide a current limiting power supply (need only a few tens of milliamperes at less than 2 volts) and proper heat sinking.

16.3.5 Electro-optics Source Testability Guidelines.

1. A laser source should be operated and stabilized prior to turning on the rest of the UUT.

2. For a DC laser with discharges, a separate current sensor should be available for each discharge.

3. Source/laser voltage should be easily measured.

4. Be able to easily check if the UUT laser/source is actually on (i.e.,lasing).

5. For a sealed UUT gas laser that is valved, gas should be easily refilled while the laser is in the system.

6. For a flowed gas laser (flowing gas not permanently sealed), the mixture should be easily sampled.

7. All optics attached to lasers should be easy to visually inspect even after installation.

8. The number of optics attached to a laser should be minimized.

9. All laser diode leads (if used) should be accessible even with their heat sinks installed.

10. "Turn-on transient circuit suppressors" should be used with diode lasers where applicable.

11. All high pressure ARC sources should be shielded from explosion due to vibration, even when cold.

12. Provide process condition monitoring (output power, overheat temperature, liquid /gas flow pressure, etc.).

13. Have the ability to monitor beam alignment, mode structure, spot size, and diameter.

14. Place ground reference on laser mirror mounts for safety during test and operation.

15. Provide ability to test with hazards removed (laser off during current regulator test, etc).

16. Provide ability to break the interface between the laser and its controller.

17. Source air cooling should be used instead of ' /ater cooling, whenever possible.

16.4 Electro-Optic Components.

Electro-optics components can include many different types of devices besides UUT optics. These include opto-isolators, solid state relays, position sensors, array detectors (such as charge coupled devices (CCDs)) image intensifiers and a variety of components used with Fiber-Optics.

Rather than to go into each of the devices separately. Some very common statements will be made in regards to UUT testability.

1. When given a choice, use flooded LEDs which include an internal diffuser making them uniformly and bright light over a large range of view angles.

2. LEDs can be driven with DC or AC while Liquid Crystal Displays (LCDs) can only be driven by an AC waveform. Attempting to drive LCDs with DC will ruin their insides.

3. When using digital circuits interfacing to E-O devices, place test points at the outputs of LED drive logic and also at inputs to optical encoders.

4. When sending signals between circuits with separate grounds, use opto-isolators or opto-couplers for isolation. These devices can provide a 2500 Vrms isolation, 10^{12} ohms insulation, and very little capacitive coupling between input and output (less than 1 picofarad).

16.4.1 Optics. There are many different types of optic materials used depending on the wavelengths implemented in the UUT. Two common materials used in Infra-Red optics are Germanium and Zinc Selenide (ZnSe). ZnSe is easier to work with since it is transparent and its internal structure can be viewed for faults. Quartz, glass, and plastics can be used for visual wavelength optics.

1. All of the above materials can be used in mirrors, regardless of the type or use such as: concave, convex and combinations lenses, prisms, beam splitters, corner cubes, gratings, and filters. It is often more economic to employ modular designs in optical modules. Modular designs consist of parts that are divided into a number of sections that can be taken out, aligned elsewhere, and then dropped back into the unit without overall unit alignment.

2. Handling of optics usually requires a clean room environment along with special handling, cleaning, and training of the test engineer in UUT alignment.

3. Electro-optic designers should minimize the number of special tools needed to align an optical UUT, and keep alignments to an absolute minimum. Ideally, automatic alignment using quadrant detectors and mechanized stages is possible but very expensive.

4. For Infra-Red (IR) modules there are other module design constraints due to the limited number of refractive materials and environmental sensitivities. These modules come in two types - reflective and refractive:

   - Reflective modules, although not suffering from chromatic aberrations, often require aspheric surfaces, are susceptible to stray radiation and may include a secondary mirror which is often difficult to align

   - Refractive modules are difficult to test due to their thermal sensitive materials, requiring expensive coatings.

5. If possible, avoid the use of germanium in a module design. Germanium is very prone to chipping and is typically bonded into a cell using a compliant RTV bond. It is visibly opaque, making it more difficult to align than ZnSe lenses. It is also impossible to visually check these components for internal flaws.

16.4.1.1 General Considerations.

1. Use prisms rather than separate optical components for proper image orientation since fewer optical parts will result in less alignment and testing times.

2. Provide a method to test aspherics independently from the rest of the module. This may require easy removal of either the surfaces or the optical assembly near it to be able to get test equipment in a confined space or to steer the beam out of the module.

16.4.2 Fiber Optics. Fiber-optics is beginning to take over more and more tasks in communications and control systems. Fiber-optics is a general term for fiber-optic cables, receivers, transmitters, connectors, and couplers. Advantage of fiber-optics include:

1. Fiber cables can share copper cable conduit trays without fear of electrical interference.

2. Fiber does not conduct electricity, so that nearby lightning strikes and the resulting power transients do not present a problem.

3. Connecting and disconnecting fiber does not produce sparks (good in explosive environment).

4. Industrial strength fiber cable has the same specs for bending conditions, temperature withstanding, etc as copper cables.

5. Crimp and cleave fiber connectors can be installed in 5 minutes and need no special skills training, or costly installation equipment.

6. Fiber-optics (F-Os) can carry 100 times more information than coax cables, plus 10 F-O cables can fit in the space equivalent to one coaxial cable.

When fibers are used in a module make sure that their cables follow one or more of the presently existing fiber standards, such as:

MIL-STD-1773:	Implementation of t nsceivers for fiber optic data bus.
ANSI X3T9.5:	Also known as the Fiber Distributed-Data Interface (FDDI)
MIL-STD-790:	Presently Under Development.
EIA FO-6	Presently Under Development.
EIA FO-2	Presently Under Development.

(Note: As of 5/11/90, the Defense Logic Agency has cancelled initial draft of DOD-STD-347, Product Assurance Program requirements for Fiber Optic Components This draft will be superseded by MIL-STD-790.)

Fiber-optics can be used for data, voice, and image transmissions. Fiber comes in many different configurations for each of the above three uses.

These configurations include large core multi-mode or small core single mode fibers (conducting many or only one wavelength). Single mode fibers allow light pulses to be transmitted at a much higher frequency due to their higher bandwidth and lower attenuation. They can further each be broken down into stepped index and graded index fibers.

Fiber-optic cables come in office grade, industrial grade, or military grade. Office grade meets the least amount of requirements and military grade meets the most number of requirements. It becomes more expensive as the number of requirements increase.

Most fiber-optics are used in Local Area Networks (LANs). There are four basic tests which need to be easily performed on fiber-optic LANs:

1. Continuity testing to basically show that fiber cables have no hidden breaks,

2. Insertion loss testing uses a power meter to measure the total loss due to fiber connections (including splices) and connectors at the nominal module operating wavelength. Use an optical power meter that reads both linear units (milliwatts) and decibels (referenced to 1 mW optical power).

3. Optical Time Domain Reflectometry (OTDR) is used to evaluate fiber loss per unit length. Usually used for cables longer than 50 meters.

4. Bandwidth testing is used to check the theoretical maximum amount of information that can be moved from A to B. This test is not recommended for multi-mode units with less than 2 Km of continuous length fiber since expensive test equipment and experienced test engineering talent must be used. A sample of a module with this much fiber is a fiber-optic gyroscope. Bandwidth tests should be performed before, during, and after fiber installation.

When checking a fiber-optic UUT, make sure that this type of raw test information is available for all fibers before and after installation and again after connections are added to the UUT. It is important that these tests be predicated on standards written by either EIA, ANSI, and/or DoD.

- Use commercially available mass termination equipment using optical interferometers to make high quality spliced connector terminations in the factory or in the field.

- Use prefocused optics at fiber-optic ends to avoid having to perform an additional alignment.

16.4.3 E-O Component Testability Guidelines:

1. All UUT optics and components (modular or not) should be easily inspected and/or replaced without damaging the optics or the UUT.

2. Designs should make provisions to direct the laser beam out of the unit without requiring the installation of optical components.

3. Use transparent optics over opaque optics whenever possible (transparent is easier to work with, example: ZnSe rather than germanium.

4. Optics should be made large enough to facilitate alignment manually and with unaided eyes so that special micrometers and microscopes are not needed.

5. Keep the number of optical elements in the optical train to a minimum.

6. Design zoom lenses to be focused without the UUT having to be turned on.

7. IR UUT image anomalies such as narcissus, scan noise, clipping, beam wander, ghosting, and shading should be easily isolated and measured.

8. Use prisms over optical components, whenever possible, so that less alignment is needed for image orientation.

9. Design the UUT so that aspherics can be tested independently.

10. Use prefocused optics at I/O ends of fiber optics whenever possible.

11. Design fiber optics so that end reflections are suppressed as much as possible.

12. Fiber-optics should be tightly coupled to minimize "coupling loss" but should also be easily removable.

13. Avoid more than one manufacturer for fiber-optic components in the same system. This will help prevent mismatches due to various connector styles.

14. Fiber-optics should conform to present standards as applicable (including EAI FO-6 and FO-2 , ANSI, and IEEE).

15. "Pyrex" mirrors should be used whenever possible.

16. Design systems to view beam direction (via video through the lens viewing) of critical and non-critical paths.

17. For fiber-optics to be used in long distance communications, use single mode reinforced fibers over multi-mode fibers wherever possible.

18. For fiber-optics to be used in image transmission, use multi-strand fibers rather than single strand.

19. All fiber-optic connectors should use an industry standard configuration. (Such as BICONIC, SMA905 & 906, ST, D4, and FC-PC).

20. Only use fibers with high numerical apertures (to improve coupling efficiency).

21. Provide coatings on optics to minimize aberrations.

16.5 Electro-Optics (E-O) Sensors and Detectors.

Detectors/Sensors form an important part of a wide range of E-O modules including Active and Passive devices. They measure the presence and intensity of electromagnetic radiation.

There are many different types of E-O Detectors/Sensors including:

- Photo-multipliers.
- Pyro-electric detectors.
- Silicon photo diodes
  - Solar cells.
  - Photo-voltaic.
  - Photo-conductive.
  - Avalanche.
- Infra-red detectors such as HgCdTe, PbS, and PbSe.

It goes beyond the scope of this handbook to describe all of these different functions other than to say that their use depends mainly on the wavelength used, design criteria, and/or the module specifications. For specific device operation, reference - The Photonics Handbook, Book II, 34th edition published by Photonics Spectra Magazine.

Some detectors (made up of thousands of elements) can take in an entire image (a mosaic or staring array) like a piece of film in a camera or they can incorporate a scanning technique (serial or parallel) permitting a small detector array (one or more elements) to have a view swept or scanned over it.

Infra-red detectors sensitive to heat have more problems that need to be tested for, especially when they have been mounted into a module.

The designer should modularize the unit in such a way as to allow checking of the detector to observe any radiation other than that from object space. These effects include narcissus, scan noise, clipping, beam wander, ghosting, and/or shading.

When choosing a detector assembly choose models that have Built-in Self Tests (BIST) if at all possible. In Oct. 1990, Opto-Electronics Textron of Petaluma California demonstrated the BIST capability for it Pbs/PbSe Infra-Red Detector Transducer. These types of devices will help increase the operational readiness in military applications since they provide easy isolation of problems.

Sensor/Detectors should be designed into a system in such a way as to be electrically removable from the circuit and allow a test signal to be injected into a pre-amplifier. By doing so, an entire system's electronics can be tested without having to go through the optical section.

16.5.1 E-O Sensor and Detector Testability Guidelines.

1. The detector should be visible through its housing (i.e., dewar container) even after installation (depending on the window material).

2. The detector assembly should be made so that the detector looks from the side whenever possible (as opposed to from the bottom).

3. The detector lens or window should be part of the detector assembly (part of the assembly means less alignment) rather than separate from it.

4. During detector alignment procedures the beam should be steered to the detector by the system optics (steering is easier) rather than moving the detector dewar.

5. The detector chip should be as large as the entrance window or larger.

6. The detector pre-amplifier should be located inside a dewar container rather than on a detector chip.

7. A temperature monitor should be installed into the dewar container as close as possible to the detector.

8. Noise Equivalent Power (NEP) should be easily measured.

9. Sensor "cool down time" should be easily measured.

10. Raw video input/output should be accessed at the sensor (i.e, such as a seeker head).

11. If a sensor is located on a stabilization system, easy access should be available to its input and output.

12. Sensor Responsivity should be easily measured.

13. The sensor should be easily electrically removed from the circuit and a test signal easily injected into the sensor pre-amp.

SECTION 17. OTHERS

17.0 OVERVIEW.

Since "others" testability covers such a wide variety of technologies, a simple set of specific guidelines cannot be developed to cover all of them. However, certain characteristics are common to many designs as follows:

For the application of the testability principles in almost all product designs:

- Develop a product that can be easily accessed and serviced at the component, module, and system level.
- Limit or eliminate manual adjustments.
- Avoid complex or excessive field testing procedures.
- Develop good Built-in-Test (BIT). (See sections 4 and 6).

17.1 Human/Hardware Interaction.

Ease of testability depends a great deal on easy, unobstructed human access to the equipment being tested. MIL-STD-1472C (Human Factors) should be consulted for specific information. Ground rules that should be considered in the design of equipment to improve testability (these may have been discussed earlier but are reiterated here for emphasis) are as follows:

1. Provide access to test points, controls, connectors, nominals, and adjustments.
2. Provide chassis slides with limit stops and cable retractors on cabinet mounted units.
3. Allow adequate space for grasping, tool or wrench clearance, and operation of adjustments.
4. Provide captive hinged access covers with quarter-turn fasteners whenever possible. Use minimum number of fasteners (when EMI is not a problem).
5. Restrict the weight of removable units to one-man lift capabilities.
6. Provide unobstructed instruction or marking labels for operating and maintenance functions. Use international instruction and warning symbols where possible.
7. Provide easily observable panel status lights to indicate status of fuses, circuit breakers, critical signals, and power.
8. Provide access openings of adequate size, which are free of sharp edges or projections so that operators in cold weather gear (heavy gloves) can maintain equipment.
9. Provide for standard tools for all maintenance or adjustments of equipment. (Special Tools must be provided and located adjacent to the function requiring them.)
10. Provide access to all UUT test points and adjustments through the UUT I/O connectors or test points for UUT functional and field maintenance testing.
11. Provide "test only" connectors for factory level testing when the primary connector is pin limited (see section 4.0).
12. Field replaceable assemblies or subassemblies should be removable without the need for unsoldering wires or unwelding sections.
13. Use light passing through a panel rather than light reflected into a panel (i.e., backlighting) for easier panel reading.

14. Provide efficient arrangement of operation and maintenance work areas, equipment, controls, and display.

15. Provide equipment with standard color coding as specified in MIL-STD-411, MIL-T-23991, and MIL-C-25050 or at least to MIL-STD-1472C.

16. Provide personnel training as necessary for both safe testing and operation.

17.1.1 Safety Provisions. Designer must eliminates or minimizes safety hazards for all maintenance, operating, and test personnel. Basic safety rules:

1. All cabinets or housings should be provided with interlocks on doors or covers to de-energize circuits upon opening.

2. For high voltage issues see section 14.

3. All radiation producing components should have shields and warning labels.

4. Provide guards or shields over moving parts (gears, chain drives, levers, etc).

5. Eliminate sharp corners and projections that could cause injuries.

6. Parts or assemblies that produce excessive temperature (over 60^{o} F) should have guards or warning labels.

7. Toxic or poisonous materials should be avoided when possible, and contained with warning labels when avoidance is not possible.

8. All power circuits should be provided with adequate safety grounds.

9. UUT must comply with latest OSHA safety standards, state safety regulations, and COMPANY safety regulations.

For further information reference latest version of MIL-STD-1472.

17.1.2 Safety And Arming (S&A) Devices. Present S&A devices must sense two (minimum) independent environments to arm the explosive train for detonation. Failure to receive or sense either environment maintains the device in the safe mode.

S&A test requirements range from 100 percent acceptance testing of individual S&A devices to testing on a lot basis, depending on type or ordinance.

The simplest S&As are pure mechanical devices; the more complex are electromechanical or completely electrical.

The most common S&A is the artillery fuse. This S&A device is passive and initiated by two dynamic environments: (1) setback and (2) spin in the gun barrel clock escapements are employed to control the time between projectable firing and arming for gun crew safety.

Some S&As use remote sensors and electronic processing to complement the passive setback sensor. The complementary sensors are used to detect barrel exit and projectile velocity. Correct parameters result in a signal to the piston actuator in the S&A to accomplish complete arming.

1. 100 % acceptance testing is required on safety and arming of nuclear weapons.

2. Each S&A device, which must sense the dynamic environment for the purposes of arming the weapon, must be tested nondestructively.

3. These devices must not contain parts that can be omitted or misassembled during the assembly operation, resulting in an armed condition.

4. S&A failure should always results in it being in a safe condition.

5. Provide visual access to critical features of assembly that must be checked for compliance.

6. The device should be able to operate in a test environment and visually indicate that it complies functionally. It should also be resetable.

7. Suitable test points for checking electromechanical actuator and sequential switches, etc., should be provided.

8. Ensure that S&A devices have obvious visual and mechanical features to alert a handler that an S&A device is in the armed position, and that is it also not possible to assemble such an armed device into a weapon system.

9. Appropriate dynamic simulators may be required for certain portions of necessary contractual testing.

17.2 Hydraulic UUTs.

Two basic types of hydraulic UUTs exists: (1) blow- down and (2) recirculating.

On a blow-down UUT, stored high pressure gas is regulated and used to pressurize an accumulator. The oil flows through servo valve actuators and is finally dumped overboard.

A recirculating UUT makes use of a DC motor pump hydraulic power supply, and oil is never exhausted overboard!

Designing testability is identical for servo troubleshooting for both types of hydraulic control systems, but different testability features are required for the recirculating hydraulic systems.

Hydraulic UUT testability guidelines include:

1. Exhaust ports for external pressure testing are required only for blow-down type UUTs. Make exhaust port one pipe size larger than the pressure port (to minimize back pressure).

2. Filters should be located in easily accessible locations for servicing. Filters, preferably of the non-bypass design, should be included internal to the pressure fitting.

3. A bypass filter should be included between the internal oil supply and the servo valves in a blow-down system to circumvent filter clogging.

4. Include visual/pressure indicator of fluid contamination level in filters without bypass features to allow for periodic inspection.

5. Access for liquid and gas test points should be through filtered and quick-disconnect ports/filters.

6. Supply DC power to all UUT amplifiers.

7. The following electrical test points should be available on a test connector for hydraulic servo testing:

   - Command input to the summing junction of the drive amplifier.

   - Position readout - generally the pick-off arm on the potentiometer.

   These test points will allow the following tests to be performed: null balance, rate, gain margin, static loop gain, polarity, and closed loop frequency response.

8. Follow all OSHA, STATE, and COMPANY safety standards as applicable.

17.3 Pneumatic UUT.

There are two types of pneumatic control UUTs: (1) the closed loop position control and (2) the open loop torque control. Either UUT can be of the cold or hot gas type when operating on its own internal gas power supply. External testing is normally performed using cold gas.

Pneumatic UUT Testability guidelines follow:

1. An external test connection for the cold gas should be located before the pressure reducing valve, which is normally an internal part of the pneumatic control system.

2. The external gas supply pressure should be internal to the pneumatic control UUT located as close as possible to the externai test connection.

3. An adequately sized filter should be internal to the pneumatic control UUT located as close as possible to the external test connection.

4. Electrical test points should be made available to provide all DC voltages necessary to energize the UUT control amplifiers.

5. External test points should be available to introduce command signals to the amplifier summing junction and to monitor control actuator position.

   (These test points will allow the following tests to be performed: polarity, rate, null balance, and closed loop frequency response.)

6. Follow all OSHA, state, and company safety standards as applicable.

17.4 Electric Drive UUT.

Electric drives are commonly employed in highly integrated configurations on missile/projectile seeker gimbals and actuators to drive ground equipment and machinery wherein separate drive system components may be used. Electric drives provide torques to rotate, elevate, slew, stabilize, and position loads in a stable mode. Electric drives utilize direct drive motors or electric motors coupled to torque multipliers (i.e., gear boxes, transmissions, ball screws, etc).

The electric drive UUTs require mechanical adjustments or measurements as well as electrical tests in an open-loop or closed-loop mode.

Electric drive testability guidelines include:

1. For transmission systems where backlash and compliance are critical, motor shafts/extensions should be accessible to enable test measurements.

2. Where mechanical adjustments are required, such as nulling of potentiometers, resolvers and gyros, component mounting hardware should be fully accessible to allow adjustment. Consideration should be given to component packaging to allow replacement of defective components.

3. Test connector(s) should be provided to enable electrical testing.

4. Electrical circuits should be designed to minimize adjustments requiring trimmers, capacitors, and nominals.

5. Floating, high voltage measurement points, which are inconvenient and dangerous, should be avoided (see section 14).

6. Test points should not be allowed to electrically/mechanically load signals.

7. Convenient ground points should be provided for probe returns.

8. Test points should appear on I/O connectors on plug-in modules.

9. In the initial design, all important signals should be brought through wiring and PC boards to the exterior of the top assembly.

10. Testing should not introduce destructive transients into sensitive circuits (use transient suppression and/or resistor buffering).

Items 3 through 8 have been repeated (from sections 2, 3, and 5) for emphasis.

17.5 BIT/BITE.

Careful consideration should be given to BITE systems (reference Sections 4 and 6). These monitoring techniques yield quick, important information as to the status at any assembly level.

BITE is most useful in measuring the following parameters:

- Over or under voltage or current.
- Power failure.
- Automatic shutdown circuits.
- High and low temperature limits.
- Circuit breaker status.
- High or low shaft speed.
- Missile hold-back latch status.

These BITE techniques and those mentioned in sections 4 and 6 can be applied to Pneumatics, Hydraulics, S&As, etc. with some creative design for testability.

17.6 Impulsive UUTs.

Impulsive UUTs impart impulse forces, with a specific thrust vector to induce corrective motions of attitude or trajectory to a controlled body. To maximize the impulse within minimum volumetric constraints, high energy density force systems are employed. Compressed cold gas, hot gas generators, deflagration propellants, and explosives may be utilized.

Testability considerations include two types of systems: (1) gas control systems, testable at the component and the system level, and (2) pyrotechnic systems, wherein control electronics are testable, but impulsive testing can be performed only by expending the pyrotechnic device itself. All these systems employ pyrotechnic devices (igniters, squib actuators, or detonators) for power source start up.

When designing testability into impulsive systems, a primary consideration is safety. Care must be exercised to prevent inadvertent firing or detonation. The effects of accidental ignition of these devices can range from the loss of expensive hardware to extreme hazards including death to personnel from explosives and resulting shrapnel.

Impulsive UUTs Testability Guidelines:

1. Provide electrical test connectors to enable UUT test.

2. Design hot gas and cold gas UUTs to incorporate an accessible cold gas external connection to enable UUT test independent of the internal power supply.

3. Consideration should be given to subsystem test of control electronics independent of associated igniters and detonators. Prior to integration with impulsive thrusting, firing circuit capacitor discharge must be ensured.

4. For propellant and explosive UUTs, if a continuity test is required for the ignition circuits, the current impressed across the igniter or detonator bridge must be well below the specified no-fire current.

5. Design safety pins or equivalent into all impulsive UUTs to preclude activation.

6. Develop required thrust and moment forces for specific time durations and operational duty cycle and provide information to test personnel.

7. Igniters and squib actuators for hot gas and cold gas UUTs should be fired from an independent circuit not associated with subsystem test.

8. Specify pyrotechnic devices with wire leads twisted and shorted. For connector interfaces, install a shorting connector.

9. Provide test equipment with protective enclosures adequate to contain discharge gases and products of combustion consistent with the UUT.

17.7 Inertial Components.

Gyroscopes and Accelerometers Testability Guidelines:

1. Electrical terminals should be identified and spaced for standard test equipment probes. Termination should consider the type of connection for ease of assembly and test (i.e., hard-wire or slip-on connector).

2. All solder type terminals must be capable of several resolders.

3. Select UUT materials so no environmental test condition (humidity, fungus, temperature) will affect testing. Eliminate corrosion, galvanic action, and leaking seals.

4. UUT design must consider the ease of installation into vibration/shock test equipment, electrical test equipment, and hardware equipment. UUT part number and test requirement specification number must be identified on an identification plate.

5. Mounting of UUT into test equipment must imitate system installation and should not affect performance (i.e., mating mounting surfaces should have the same surface finish, tolerances, and indexing as system installation).

6. Gyroscopes and accelerometers incorporated into inertial UUTs must be accessible for alignment (nulling) and test probes. UUTs must be located for ease of replacement and test. Provision should be made for centralized terminal boards and easily replaced UUT locking hardware.

7. A decal illustrating a simplified circuit diagram and reference to a system specification must be provided.

8. Self-test features (BITE) must be provided (i.e., spin motor rotor detection circuit to detect run-up speed of the inertia wheel of a gyroscope) (see sections 4 and 6).

9. Vacuum or gas-driven gyroscopic UUTs should allow for speed adjustment and have provisions for sense points through quick-disconnect fittings in a way that will not introduce contamination.

17.8 General Mechanical Components.

Many mechanical UUTs and mechanisms are designed to perform specific functions such as control, drive, rotate, elevate, monitor, move, restrain, and release using electrical torque motors, electrical solenoids, hydraulic driven motors, pneumatic actuators, hydraulic, pneumatic, and hot gas valves, etc.

Special components that are designed from a concept or are modified from available items must have designed-in testability features for bench acceptance and workmanship testing. The design requirements or specification for the UUT will describe the particular functions critical to the design use and will be the basis for establishing the design testability features.

The following guidelines are presented for general use in the design process.

17.8.1 Testability Of Structural Elements. The ability to perform load-bearing functions is normally validated by inspection, test, and analysis prior to UUT use. Structural methods, whether consisting merely of a visual check or more elaborate methods, are a part of the specification/testability tradeoff process and will affect the life cycle costs of a system.

Mechanical Testability Guidelines:

1. Minimize the need for testing by providing adequate structural margins to preclude strength proof testing or need for field replacement.

2. Provide structural members with simple visual verification of their load-bearing strength capabilities.

3. Standardized functional components with well-established strength values should get only lot verification testing. This applies to threaded fasteners, pins, wire, rope, and latches as well as structural shapes.

4. Material property testing should be avoided or limited to pre-production or in-process validation of material strength.

5. Scale down in-process testing of structural elements to a limited sampling basis after the production process (weld, heat, dip braze, casting, etc.) has been validated.

6. If acceptance validation is required on a structural member, a non-critical portion of the member should be designed for hardness check or inspection.

7. If field inspections are necessary due to personnel safety or system operation failure, the following guidelines should be observed:

   a. Provide visual inspection of structurally critical areas and deformation zones.

   b. Avoid material property checks or limit to simple hardness checks.

c. Provide convenient load points and avoid simplifying any part removal procedures.

d. The need for special (non-axial) load application setups should not be specified. Proof test results must be documented to eliminate the need for repeated validation testing.

e. Avoid heavy hoisting equipment which requires high safety factors, provisions for proof testing, and removal of each determinant load-carrying element.

f. The verification of material physical properties must be maintained by a traceable paper trail to a verification source. Testing verification records are normally provided by the vendor supply source.

g. Observe all OSHA, state, and/or company standards as applicable,

17.8.2 Gear Boxes And Pulley UUTs.

These UUTs should be designed so that stub shafts and input/output shafts can be used for speed and torque measurements for factory acceptability or qualification testing. Field testing at specified intervals can indicate operational changes as a function of life; backlash and no-load torque measurements can also use these test points.

These guidelines should be used:

1. The shafts and other test points should be designed to detect changes in UUT performance, dictating a necessary overhaul.

2. Lubrication UUTs must provide access for oil sampling to detect foreign particles, contamination, breakdown, or viscosity changes.

3. Gear UUTs, particularly adjustable ones, should be provided with access covers to enable periodic tests of backlash at intermediate points, as well as input to output. Backlash measurements are used to reset adjustable gears or to determine the rebuild life of fixed UUTs.

4. Chain, cable, rope, and strap UUTs are subject to wear and require periodic visual checks for frayed, chipped, cracked, or worn components.

5. Periodic proof load testing is required in critical UUTs that could produce a hazardous situation if failure occurred.

6. Hoisting UUTs, especially those used to handle ordinance, should be periodically tested at twice the maximum load.

7. Observe all OSHA standards as required including state and factory safety standards.

8. Access panels should exist for visual and mechanical access to critical components and components subject to wear such as engine mounts, wing struts, chain, and ropes.

17.9 Software Testability Guidelines.

There are two types of software which can be discussed when talking about testability. The first type is used to run the system/UUT to perform its specified mission function and the second is used in internal or external test of the UUT itself..

Both software types have the same general design guidelines for testability.

In this case testability of the software refers to how easy it is to verify, debug and maintain both software and documentation during a UUTs life time evolution and/or changes in UUT specifications.

Using a military standard much as MIL-STD 2167 and/or company standard can greatly aid in software development for maintenance/testability..

17.9.1 Software Development Plan (SDP). The SDP contains information for development and maintenance of the software (being made up of one or more documents) over its entire development lifetime. This SDP document should provide but not be limited to:

1. To formerly verify software performance and provide a Software Requirement Specification (SRS).
2. Provide a separate Software Acceptance Test Plan (SATP).
3. Provide a Flow Diagram (FD) for both the system and test software packages.
4. Provide a Regression Test Baseline (RTB) to reconfirm software integrity following software maintenance actions.

17.9.2 General Software Testability Guidelines.

1. Program with Maintenance/Verification in mind.
2. Do not generate self modifying code!
3. Use only one program source statement.
4. Do not use complex loop structures.
5. Do not use lengthy program source statements.
6. Define all variables in each subroutine.
7. Design all Software/Firmware in a modular top down structure with comments.
    a. Provide for organized/modularized programs and data.
    b. Standardize header, test name, and data base items.

c. Pass as few data items between modules as possible.

d. Provide Software Quality Assurance (SQA) and Configuration Management (CM) procedures.

e. Besides providing code commenting, formatting, and identification, also provide Software description documentation with flow diagrams.

f. Use a principle Generic Program Design Language (PDL) in the form of structured English before actual coding so it can be easily discussed by hardware and software engineers alike.

g. Review all documentation including Program Design Language (PDL) before Critical Design Review (CDR) and before coding starts.

17.9.3 Software Testing. After a module of a larger piece of software (S/W) has been coded, compiled and/or assembled error free, and reviewed, it can enter the test phase which is broken down into 3 parts: (1) Unit Test, (2) S/W integration Test, and (3) UUT test.

17.9.3.1 Software Unit Testing. Use the test plan and related documentation. The unit should exercise the module exhaustively to shake out any bugs. This test is performed in a simulator or if possible "actual" test environment. Trace program tools are very helpful for this type of testing. If test software tools are developed in parallel with UUT software this step can be performed faster.

17.9.3.2 S/W Integration Test. Once many modules have completed software unit testing they can be integrated into one large design and again thoroughly tested for module integration bugs. In this test, controlled S/W halts at breakpoints providing for patching capabilities are helpful. These are as important as program audit trails and data collection methods. All test results should be stored in a Test Results Document (TRD).

17.9.3.3 UUT Test. Once a software program has been tested using Software Unit Test and S/W Integration Test, it is ready to be tested with the "real" hardware configuration.

Here problems will crop up between the original "simulated" hardware and the "actual" hardware for which software changes have to be made and documented.

17.10 General "Other" Testability Guidelines No: Covered Elsewhere.

The following guidelines are presented for general use in the design process:

1. All electrical devices should have standardized color-coded wires. In addition, terminals on the parts should be labeled or coded.

2. All electrical devices that have wire leads should allow extra length of wire for test soldering if required, or assembly or disassembly if a component malfunctions.

3. All electrical devices should be marked with an appropriate index for orientation relative to its use.

4. All electrical devices should be bench-mounted similar to the actual applications to allow for equivalent heatsinking and clamping forces.

5. Flow devices, whether hydraulic, gas, or pneumatic should have input/output ports clearly marked for bench testing. The requirements for filters and electrical energy, as necessary, should be provided at appropriate points.

6. Position measuring devices (potentiometers) should have accessible leads for resistive measurements and a mechanical output shaft or level for calibration and coordination of the mechanical versus the electrical relationship. Positive and negative directions relative to actual positioning should be noted on the output mechanisms.

7. Inner and outer races of bearings are generally adequate when tested with appropriate fixtures in a dynamometer. However, special bearings with very thin races, which utilize the mounting structure for support and stiffness, should be avoided. Since many precision bearings have run-in and spin-up/spin-down requirements, races should be adequate for strength, stiffness, and dimensional stability.

8. All nondestructive testing methods and criteria such as magnaflux, ultrasonic, and eddy currents should be specified as required. Material defects such as scratches, gauges, and surface cracks should be defined to maximize yield during fabrication and maintenance.

9. Seals should be tested in supporting fixtures duplicating the actual installation. In general, seals are not 100% tested, but when installed in a system, the system may be subjected to proof test.

10. Universal joints and couplings can usually be tested by appropriate fixtures that simulate the installation. Environmental controls consisting of fans, heaters, and/or air coolers are self-contained items, but should be designed for bench testing by having appropriately marked test connectors with test plates suitably labeled. Units requiring cooling liquids should have fill and drain ports marked, and labels with call-outs for quantity and class of fluid with any cautions should also be suitably marked.

11. Provide a UUT with visual and audible non-bypassable alarms when critical control or control combinations are manually set to unsafe limits.

12. Avoid the need to modify a UUT in any way to perform a test.

13. Provide test point access and adjustment capabilities without being able to introduce contamination in the rest of the UUT (dust, dirt, air, moisture, etc.).

14. Locate external temperature monitoring test points before the pressure reducing valve to get "actual" UUT temperature.

15. Use VLSI digital synchro/resolver tachometers (since they are less expensive and more reliable) whenever possible.

16. Air flow UUTs should use a filter/regulator/lubricator as a single package module where possible to cut down the number of units which need to be tested and or replaced. A single unit is often less expensive than three separate units.

BIBLIOGRAPHY

BIBLIOGRAPHY

Agrawal, V. D., K. T. Cheng, D. D. Johnson, & T. Lin, "Designing Circuits with Partial Scan," IEEE Design & Test of Computers, April, 1988

Alfaro, K., "LSI Adds JTAG to Can Cells," Electronic Engineering Times, October 9, 1989

Allingham, D., & D. Vendl, "It's Easy to Get Trapped by Simulation-to-Test," High Performance Systems, August 1989

Andrews, W., "GaAs ICs Begin to Make Inroads in Silicon Territory," Computer Design, February 1988

Avra, L., "A VHSIC ETM-Bus-Compatible Test and Maintenance Interface," IEEE International Test Conference, 1987

Banks, S. M., "Getting Started in TAB," Surface Mount Technology, August 1989

Barrow, J., "Avoiding Ground Problems in High-Speed Circuits," RF Design, July 1989

Bennetts, R. G., Design of Testable Logic Circuits, Addison-Wesley, London, 1984 (Microelectronics Systems Design Series).

Besser, L., & D. Davis, "Dick Anderson of HP on Trends in Microwave ATE and CAE," Microwave Systems News, May 1987

Bhawmik, S., et al., "DFT: Expert: Designing Testable VLSI Circuits," IEEE Design & Test of Computers, October 1989

Binnendyk, F., & S. Rutherford, "Why the Push is on to Merge Design and Test," High Performance Systems, August 1989

Blecha, J. F., "Testability Planning for Improved System Performance," IEEE AUTOTESTCON, 1988

Borden, A. G., "The Impact of Advanced Computer Systems on Avionics Reliability," Defense Electronics, May 1987

Boyle, D., "Gallium Arsenide, Microwave Technology Firming Up," Defense Electronics & Computing, May 1989

Boyle, L., "Pave Pillar: a New Road to Avionics Reliability," Interavia Aerospace Review, 1983

Brothers, P., et al., "Level Testing 100K ECL Demands Attention to Detail," Electronics Test, March 1987

Bullock, M., "Designing SMT Boards for In-Circuit Testability," IEEE International Test Conference, 1987

Bursky, D., "New ECL GaAs ICs Heat Up the High Speed Race," Electronic Design, October 13, 1988

Carrbil, M. P., & G. W. Peterson, "In-circuit Tester Takes on ECL, TTL, and MOS Devices,"Electronic Design, May 28, 1981

Carrol, M., "Built-in Array Payoff; Better Fault Detection," High Performance Systems, August 1989

Cole, B. C., "Boosting Density in a 2-Micron Process," Electronics, February, 1989

Cole, B. C., "Now Power-Saving GaAs Equals ECL Density," Electronics, February, 1989

Cole, B. C., "Now There's More Than Just Raw Speed in the ECL Arena," Electronics, February 1989

Collett, R. E., & P. W. Bachant, "Integration of BIT Effectiveness with FMECA," IEEE Reliability and Maintainability Symposium Proceedings, 1984

Comerford, R., "CAE Delivers Alternatives for Testing Complex Boards," Test & Measurement World, October 1989

Condom, P., "Combat-Ready Electronics, IFTE Takes the Field," Defense Electronics & Computing, May 1989

Cooper, L. J., & D. E. Smith, "Reasoning From Uncertain Data: A BIT Enhancement," IEEE AUTOTESTCON, 1989

Crosby, B. C., "ECL Board Testing: An In-Circuit Point of View," IEEE International Test Conference, 1982

Curran, L., "Scalable System Concept Hits ATE," Electronics, November 1989

Curran, L., "Wafer-Scale Integration Arrives in "Disk" Form," Electronic Design, October 26, 1989

Damm, W., "ASIC Verification: How Much is Enough?," Electronics Test, September 1989

Daugherty, D. W., "A New Approach to Design for Test Improves Fault Coverage," Electronics Test, September 1989

Daugherty, D. W., "Electronics Test Automation Aids In-Circuit Test," Electronics Test, July 1989

Daugherty, D. W., "Making Surface-Mount PCB's Testable," Electronics Test, June 1989 IEEE AUTOTESTCON, 1987

Daugherty, D. W., "Software Takes the Sting Out of Functional Test Development," Electronics Test, August 1989

Davis, R., "Focus Report: Hogh Speed ASIC Competition Heats Up," ASIC Magazine, September 1989

Dervisogru, B. I., Scan-Path Architecture for Psuedorandom Testing," IEEE Design & Test of Computers, August, 1989

Desena, A., "DOD Drafts Integrated Diagnostics Into Service," Computer Design, April 1, 1988

De Simone, S. E., "Test Technique for ECL Loaded Boards," Computer Design, June 1982

Dhillon, P., "Understanding RF/Microwave ATE Switching," Tutorial, Microwave Systems News, August 1989

Droste, D., "Testability: The State of the Art, Automatic Testing in the Next Decade & the 21st Century," IEEE AUTOTESTCON, 1989

Dunn, P., "Boundary Scan Technique Stimulates Gear, Pack Firms as Standard Nears," Electronic News, September 1989

Durwood, B., & D. Pellerin, "PECs Are a New Addition to the ASIC Family Tree," ASIC Magazine, September 1989

Eden, R. C., et al., "Integrated Circuits: The Case for Gallium Arsenide," Spectrum, December 1983

Evanczuk, S., "IEEE 1149.1: A Designer's Reference," High Performance Systems, August 1989

Farrell, T., P. Hurrle, "Spread Spectrum Systems, Test Requirements, & Maintenance," IEEE International Test Conference, 1985

Fasang, P.P, D. Mullins, & T. Wong, "Design for Testability for Mixed Analog/Digital ASICs," IEEE Custom Integrated Circuits Conference, 1988

Feindel, D., "COB and TAB: Evaluating the New Assembly Technologies," Surface Mount Technology, August 1989

Fichtenbaum, M. L., "A Memory Test Approach for the General Purpose Digital Board Tester," IEEE International Test Conference, 1987

Fleming, P., "Expanding Beyond Boundary Scan Techniques & JTAG," IEEE WESCON 1988

Franco, J. R. Jr., "Experiences Gained Using the Navy's IDSS Weapons System Testability Analyzer," IEEE AUTOTESTCON, 1988

Franco, J. R. Jr., "WSTA - The IDSS Weapon System Testability Analyzer," IEEE AUTOTESTCON, 1987

Friedley, D. P., "Better Test Tools are Needed for the '90s," Electronic Engineering Times, August 7, 1989

Fujiwara, H., "Design for High-Speed Testability," IEEE International Test Conference, 1987

Funatsu, S., M. Kawai, & A. Yamada, "Scan Design at NEC," IEEE Design & Test of Computers, June 1989

Gallant, J., "GaAs Digital ICs Complement ECL Families in High Speed Applications," EDN, March 3, 1988

Gambino, K., & J. Prang, "Design-Test Link Software," Evaluation Engineering, October 1989

Gambino, K., & J. Kenney III, "Make Your surface-Mount PC Boards Testable," EDN, October 12, 1989

Gillespie, D. W., K. D. Wilkinson, & B. Merrell, "BIT & Testability for Millimenter Wave Systems, IEEE AUTOTESTCON, 1989

Ginsberg, G. L., "TAB Enters Multichip Modules for the Next Step in High Density Packaging," Electronic Packaging & Production, September 1989

Goel, P., "Design for Testability, an Opinion," Electronics Test, December 1985

Goodenough, F., "Analog System Design," Electronic Design, January 1, 1989

Gosch, J., "At Last, A Standard On-Chip Test Bus, " Electronics, October 1988

Griffin, K., "VHSIC Phase 2 Test Requirements for the Depot," IEEE AUTOTESTCON, 1989

Haight, J., "GaAs Logic Characteristics Results in Integration Problems," EDN, June 28, 1984

Hallenbeck, J. J., N. Kanopoulus, N. Vasanthavada, & J. W. Watterson, "CAD Tools for Supporting System Design for Testability," IEEE International Test Conference, 1988

Hallenbeck, J. J., J. R. Cybrynski, N. Kanopoulos, T. Markas, & N. Vasanthavada, "The Test Engineer's Assistant: A Support Environment for Hardware Design for Testability," IEEE Computer, April 1989

Halliday, A., G. Young, & A. Crouch, "Prototype Testing Simplified by Scannable Buffers and Latches," IEEE International Test Conference, 1989

Hansen P., C. Rosenblatt, "Handling the Transition to Boundary Scan for Boards," High Performance Systems, August 1989

Hansen, P., "Testing Conventional Logic and Memory Clusters Using Boundary Scan Devices as Virtual ATE Channels," IEEE International Test Conference, 1989

Hansen, P., & T. Borroz, "Tough Board Test Problems Solved With Boundary Scan," Electronics Test, June 1989

Hemink, G. J., H., G., Korkhoff, & B. W. Meijer, "TASTE: A Tool for Analog System Testability Evaluation," IEEE International Test Conference, 1988

Henderson, B. W., "Boeing Achieves Match Advance in Space Solar Cell Efficiency," Aviation Week and Space Technology, October 23 1989

Henley, F. J., "Application of Electro-Optic Techniques to Integrated Circuit Testing," SPIE- Int. Soc. Opt. Eng. Proceedings, Vol. 774, pp. 57-61.

Henning, C. G., " Spread Spectrum Test Criteria and Methods," IEEE AUTOTESTCON, 1984

Hess, R. D., "Considerations in Selecting a Design-for-Testability Technique," IEEE AUTOTESTCON, 1988

Hines, R., "Using Space to Debug Test Hardware," Electronics Test, August 1989

Hobson, L., "Interconnecting Multichip ICs in a Plastic Package," Electronic Packaging & Production, September 1989

Hogan, W., M. Spellman, "ATE Test of Spread Spectrum Systems," IEEE AUTOTESTCON '82, pp. 385-92.

Huisman, L. M., et al., "The Reliability of approximate Testability Measures," IEEE Design & Test of Computer, December 1988

Irwin, H. R., "A Brief History of Microwave ATE: 25 Year of Progress," Microwave Systems News, May 1989

Iscoff, R., "How ASICs Become Systems," ASIC Magazine, September 1989

Jackson, C. K., "Electromagnetic Compatibility of Spread Spectrum Communications Systems," IEEE International Symposium on Electromagnetic Compatibility, pp. 217-20.

Jarwala, N., & C. W. Yau, "A New Framework for Analyzing Test Generation and Diagnosis Algorithms for Wiring Interconnects," IEEE International Test Conference, 1987

Jaszka, P. R., "Industry Adapts to Meet Military ATE Requirements," Defense Electronics, September 1989

Johnson, D., & S. Quinn, "Applied Power-Board Testing," Powertechnics Magazine, October 1989

Jones, K. E., E. W. Strid, & K. R. Gleason, "mm-Wave Wafer Probes Span 0 to 50 Ghz," Microwave Journal, April 1987

Jordan, S. C., "Hou Automated Test & Measurement Makes Ultra-Precision Electro-Optic Applications Affordable," IEEE WESCON, 1988

Judge, K. C., "Two-Level Maintenance Concept for Advanced Avionics Architecture," IEEE AUTOTESTCON, 1989

Kakani, T., "Testing of Surface Mount Technology Boards," IEEE International Test Conference, 1987

Kanopoulos, N., N. Vasanthavada, J. Watterson, & J. J. Hallenbeck, "A New Implementation of Signature Analysis for Board Fault Isolation Testing," IEEE International Test Conference, 1987

Karalikas, N., "Electro-Optical Test Facility Comcept & Program Review," IEEE AUTOTESTCON, 1986

Karalekas, N., S. Millender, R. Priddy, & J.Zollo, "Testability of Electro-Optical Systems," IEEE AUTOTESTCON, 1987

Kelly, G., "Single Point TAB- A Bonding Solution for High Density Chips," Surface Mount Technology, August 1989

Klos, L., "Pave Pillar Avionics - An Architecture for the Future," IEEE NAECON, 1984

Konemann, B., & K. Wagner, "Practical BIST: Old and New Tools in Concert," IEEE Design & Test of Computers, August, 1989

Kroft, D., "A Standard Method to Increase the Testability of OCMS (the BIBLO) of VLSI-6000 Technology and All Pseudo-Fault Injection," First International Conference on Computer Technology Proceedings, COMPEURO, 1987

Landis, D. L., "A Self-Test System Architecture for reconfigurable WSI," IEEE International Test Conference, 1989

Langley, F. J., R. R. Boatright, & L. Crosby, "Composite Electro-Optical Testing of Surface-Mount Device Boards - One Manufacturers Experience," IEEE International Test Conference, 1989

Leanard, M., "Digital System Design," Electronic Design, January 1, 1989

Leanard, M., "GaAs Technology Advances on Multiple Fronts," Electronic Design, October 12, 1989

Leanard, M., "IC Fabrication Techniques Sculpt Silicon Sensors," Electronic Design, October 26, 1989

Lee, J. H. & W. E. Stark, "Modeling and Test Patterns for Frequency-Hopped Spread Spec rum Systems," Tencon '87 Conference, Seoul 1987

Levy, A., "Industrial Testability Standaras Fits Military Applications," Electronic Products, October 1989

Liu, D. L., & E. J. McCluskey, "Designing CMOS Circuits for Switch-Level Testability," IEEE Design & Test of Computer, August 1987

Longendorfer, B. A., "A Testability Measure for Hybrid Circuits," IEEE International Test Conference, 1979

Loveless, R. M., "Tailoring Integrated Diagnostics Requirements to Reduce Weapon System Program Risks," IEEE AUTOTESTCON, 1986

Ludvigson, M. T., & K. L. Milton, "High Speed bus for Pave Pillar Applications," IEEE National Aerospace and Electronics conference, 1985

Lyman, J., "Component & Packaging," Electronics Design, January 1, 1989

Magnus, S. A., "Two JTAG Test Boards Plug Into PCs," EDN, October 5, 1989

Malcolm, J. G., & G. L. Foreman, "The Need: Improved Diagnostics Rather Than Improved R," IEEE Reliability and Maintainability Symposium Proceedings, 1984

Malik, S., & L. Jorstad, "Testing for CMOS Latch-up Immunity," Electronics Test, July 1989

Margolin, B., "Power Supply Testers and Leads," Powertechnics Magazine, July 1989

Markstein, J. W., "Electronic Packaging for the Military Environment," Electronic Packaging & Production, September 1989

Matsuda, Y., K. Arimoto, M. Tsukude, T. Oishi, & K. Kujishima, "A New Array Architecture for Parallel Testing in VLSI Memories," IEEE International Test Conference, 1989

Maunder, C., & F. Beenker, "Boundary Scan - A Framework for Structured Design-for-Test," IEEE International Test Conference, 1987, pp. 714-23.

Maunder, C., "The Joint Test Action Group," Computer-Aided Engineering Journal, August 1986

Mazumder, P., & J. H. Patel, "An Efficient Built-In Self Testing for Random Access Memory," IEEE International Test Conference, 1987

McClean, D., S. Banerji, & L. Whetsel, "Bringing 1149.1 Into the Real World," High Performance Systems, August 1989

McClean, D., & J. Romeu, "Design for Testability with JTAG Test Methods," Electronic Design, June 1989

McClusky, E. J., Logic Design Principles, Prentice Hall, New Jersey, 1986

McDonald, Jo Ann, "What's Behind the MIMIC Program?," Microwave Systems News, September 1989

McLeod, J., "ASIC Testing Just Got Easier," Electronics, August 1989

McLeod, J., "Bringing Down the costs of ATE," Electronics, November 1989

Menozzi, G. "Large Scale Interconnects for Aerospace Applications," Sixth European Microelectronics Conference, June 1987

Merlino, D. H., & J. Hadjlogiou, "Built-in Test Stategy for Next Generation Military Avionic Hardware," IEEE International Test Conference, 1989

Miller, C. D., "VLSI Design for Fault-Dictionary Based Testability," IEEE AUTOTESTCON, 1988

Milne, B., "Testability," Electronic Design, January 10, 1985

Modrow, M. B., "High Speed Databus for the Air Force," Avionics, March 1989

Morgan, D. R., "Pave Pace: system avionics for the 21st Century," IEEE AES Magazine, January 1989

Novellino, J., "Embedded Structure Tests ASICs Fully and Easily," Electronics Design, July 13, 1989

Novellino, J., "VLSI Technology Squeezes Tester Onto One Chip," Electronics Design, July 27, 1989

Papczynski, R. J., "Improving Manufacturability With Good SMT Design Practice," Surface Mount Technology, August 1989

Park, E. S., & M. R. Mercer, "Robust and Nonrobust Tests for Path Delay Faults in a Combinational Circuit," IEEE International Test Conference, 1987

Parker, K. P., "Testability: Barriers to Acceptance," IEEE Design & Test of Computers, October 1986

Parker, K. P., "The Impact of Boundary Scan on Board Test," IEEE Design & Test of Computers, August, 1989

Parker, L., & R. Koelling, "ASICs Provide Built-in Test Capability," Electronics Test, September 1989

Pascente, J. E., "X-Ray Maxes Instant in Line TAB Inspection Possible," Electronic Packaging & Production, September 1989

Pearson, T. J., "Advanced "ECL" Logic Bridges Gap Between GaAs and Existing Silicon Logic," IEEE WESCON 1988

Pivin, D., "Built-in Self-Test: The Role of BIST and DFT in Gate Array-Based Digital Designs," Evaluation Engineering, November 1989

Prang, J. A., "Where the Probe Meets the Pad: Designing Testable SMT Boards," Electronics Test, September 1989

Pyron, C., & R. Sallade, " CAE Functionality for Verification of Diagnostic Programs," IEEE International Test Conference, 1989

Quinnell, R. A., "Mixed Analog-Digital ASICs," Electronic Design News, June 22, 1989

Ramseyer, R. R., & D. T. Lee, "Strategy for Testing VHSIC Chips," IEEE AUTOTESTCON, 1982

Ratiu, I. M., A. Sangiovanni-Vincentelli, & D. O. Pederson, "VICTOR: A Fast VLSI Testability Analysis Program," IEEE International Test Conference, 1982

Render Sr., N. G., "Designing for Testability in this VHSIC Environment," IEEE AUTOTESTCON, 1986

Rhines, W. C., "Testing Becomes a Concern for Semi Houses," Electronic Engineering Times, August 7, 1989

Rhodes, L., "Intelligent Instruments Take Burden Out of Microwave Test," Microwave Systems News, May 1989

Robinson, P., "Gallium Arsenide Chips," BYTE, November 1984

Robinson, R., "Improving the Testability of SMT Boards," Electronics Test, July 1989

Rosales, B. C., "Test and Synthesis: A Critical Coupling," High Performance: Semiconductor Design Guide, 1989

Rosen, C., "Microprocessor Outlook," Electronics Purchasing, July 1989

Roskell, D., "Boundary Scan Leads to Better Fault Finding," New Electronics, Nov. 1988

Runyon, S., "Credo for a New Decade: Design for Testability," Electronic Engineering Times, August 7, 1989

Runyon, S., "Designers Wait for Tools to Forge Design-to-Test Links," Electronics Engineering Times, August 14, 1989

Runyon, S., "Growing Legions of Faithful Take DFT to Heart - and the Fab," Electronic Engineering Times, August 7, 1989

Runyon, S., "There's Plenty of Activity in the Mixed Signal Arena," High Performance, August 28 1989

Runyon, S., "Standards, Software Lend Design Status to Test," Electronic Engineering Times, August 21, 1989

Sarkany, E. F., & W. S. Hart, "Minimal Set of Patterns to Test Ram Components," IEEE International Test Conference, 1987

Savaria, Y., & B. Kaminska, "Force-Observe, A New Design for Testability Approach," IEEE ISCAS Proceedings, 1989

Scheilber, S. F., :"Determining Analog-System Testability," Test & Measurement World, October 1989

Sharma, A. K., & R. K. Ellis, "Reduce MMIC Production Costs Using Integrated Testing and Modeling System," Microwave Systems News, July 1989

Sheil, B., "Programming the Uncertain with Exploratory Systems," Computer Design, March 1985

Sherman, D. E., "Testability Using LOGMOD," IEEE AUTOTESTCON, April 1989

Shirley, M., P. Wu, R. Davis, & G. Robinson, "A Synergistic Combination of Test Generation & Design for Testability," IEEE International Test Conference, 1987

Shroen, W., & S. Malhi, "3-D Packaging Spawns Smaller, Faster Systems," Surface Mount Technology, August 1989

Spitzer, C. R., "Making Maintenance Easier," Avionics, July 1988

Stenbakken, G. N., "Ambiguity Groups and Testability," IEEE Transactions on Instrumentation and Measurement, October 1989

Stephenson, J. E., "A Testability Measure for Register Transfer Level Digital Circuits,"

Stora, M. J., "A New Approach to Military ATE," Test & Measurement World, June 1985

Stroud, C. E., & A. E. Barbour, "Design for Testability and Test Generation for Static Redundancy System Level Fault-Tolerant Circuits," IEEE International Test Conference, 1989

Thorel, P., R. David, J. Pulou, & J. L. Rainard, "Design for Random Testability," IEEE International Test Conference, 1987

Trivedi, M. M., "Present and Future Directions: Trends in Artificial Intelligence," Optical Engineering Reports, September 1989

Tsui, F. F., LSI/VLSI Testability Design, McGraw Hill, New York, 1987

Turino, J., "IEEE P1149 Proposed Standard Testability Bus -- an Update with Case Histories," IEEE International Test Conference, 1988

Turino, J., "Interfacing to Boundary Scan Chips for System Level BIT," IEEE AUTOTESTCON, 1989

Turino, J. L., "Testability Recognized as an Important Factor to User and Vendors," Evaluation Engineering, November 1984

Turino, J. L., "There's Room for Multiple Test Techniques," Electronic Engineering Times, August 21, 1989

Turner, C. F. "Integrated Systems," IEEE Potentials, Feb. 1988

Tustin, W., "Environmental Stress Screening: What's Happening?," Evaluation Engineering, October 1989

Vasanthavada, N., & N. Kanopoulos, "A Built-in Test Module for Fault Isolation," IEEE Design & Test of Computers, June 1989

Vereen, L., "Board Tester Supports Boundary Scan," Electronics Test, June 1989

Vereen, L., "Combinational Testers: Everything but the Kitchen Sink," Electronics Test, June 1989

Wagner, K. D., & T. W. Williams, "Design for Testability of Mixed Signal Integrated Circuits," IEEE International Test Conference, 1988

Walsh, D. A., "Linking Design to In-Circuit Board Test," Electronic Test, June 1989

Weber, S., "Analog Gets Automated," Electronics November 1989

Weber, S., "Computer Aided Testing Gets Real," Electronics, November 1989

Weber, S., "Looking Ahead to FDVDI," Electronics, November 1989

White, D., "Using Analog Sampling and Digital Storage to Improve ECL Testing," Electronics Test, April 1984

Wittenberg, R. C., Scanning and Sampling," Electronic Engineering Times, October 9, 1989

Wong, T. S., "Next generation bipolar "ECL" Technology produces ultra-fast ECL RAMs," IEEE WESCON 1988

Zourides, V. G., "Smart Built-in-Test (BIT) An Overview," IEEE AUTOTESTCON, 1989

"3-D Packaging Saves Board Area, Uses Wrap Around Flex," Electronic Packaging & Production, September 1989

"Adapter Simplifies ECL Device Testing," Microwave & RF, November, 1987

"Avantek Pursues Separate MIMIC Strategy Rather Than Participate in Pentagon's Program," Aviation Week & Space Technology, September 18, 1989

"Computers Review," Defense Electronics & Computing, May 1989

"Designing High-Quality Test Vectors for ASICs," High Performance: Semicustom Design Guide, 1989

"Extended Serial Digital Signal (ESDS) Subset Testability Bus Protocol and Implementation Specification," IEEE-STD-P1149.2-1989/D2

"In-Circuit Tester Takes on ECL, TTL, and MOS Devices," Electronic Design, May 28, 1981

"Military Systems Use New Communications Technologies," Aviation Week & Space Technology, October 30, 1989

"MIMIC Rolls On, But Cost Still High," Microwave & RF, September 1989

"Radar Review," Defense Electronics & Computing, May 1989

"Raytheon/TI Aim at High-Volume MMIC Chip Production Capacity," Aviation Week & Space Technology, September 18, 1989

"Standard Test Access Port and Boundary-Scan Architecture," IEEE-STD-P1149.1/D5 (JTAG), IEEE Computer Society, June 20, 1989

"Verification Tool Handles Mixed-Signal Chips," High Performance Systems, August 1989

IEEE Standard for a Testability Bus, sponsored by Test Technology committee of the IEEE Computer Society, IEEE-STD-P1149-1989D8, 1989

MIL-STD-2165, "Testability Program for Electronic Systems and Equipments"

MIL-STD-454; Requirement 1, "Safety Design Criteria - Personnel Hazards"

NAVMAT P-4855-1A (NAVSO P-3641).

NFPA 70 and NFPA 70E-1979.

OSHA 55 FR31984.

Generic Integrated Maintenance Diagnostics (GIMADS) Designing Weapon Systems with the Maintainer in Mind," Draft U. S. Air Force Guide Specification, August 1990

Generic Integrated Maintenance Diagnostics (GIMADS), Draft Air Force Military Standard, August 1990

GLOSSARY

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Ad-Hoc Test Approach — Add control and visibility points after initial design.

Structured Test Approach — BIST, Scan Chain, LSSD, etc.

Ambiguity Group — The group of maintenance replaceable units which have faults resulting in the same signature.

Asynchronous — The existence of circuit activity occurring which is not dependent on a reference clock signal.

Availability — The fraction of time that a system is available for use.

Backplane — A motherboard used to connect module I/O connectors together for inter-module busses and signals.

Bayesian Process — A statistical process using prior information.

Bit — One binary digit.

Boundary Scan — A structured testability approach designed into an IC's circuitry.

Built-in Test — A capability of equipment to automatically detect failures within itself.

Cannot Duplicate — A reported operational system fault that cannot be duplicated at the organizational level of test

Clock — A signal used to synchronize and initiate functions and other signals in an electronic design.

Cluster Test — Term used in incircuit testing when more than one device are tested simultaneously.

Combinational circuit — An electronic circuit with an output which is dependent on its present input signal states only. Its output is not dependent on any previous signals or states.

Component — A physical piece of hardware.

Controllability — The degree to which a signal may be driven to specific states or values during test.

Diagnostics	Detecting faults after they occur.
Failure	The state of inability of an item to perform its required function.
False Alarm	A BIT indication or report of a fault where no fault exists.
False Alarm Rate	The rate at which false alarms occur.
Feedback Loop	The circuit loop which exists when a circuit output signal re-enters the circuit as an input.
Functional Test	A test technique where a tester manipulates and monitors normal signals from the UUT I/O connector.
Glue Logic	Components used to tie VLSI and VHSIC logic together.
Hamming Code	A linear block code that can be used to detect or correct errors during data transmission.
Hybrid	A combination of two or more technologies on one device, module, or board.
Incircuit Test	A test technique where test equipment simultaneously accesses each node in a circuit card so that individual components can be tested.
Initialization	The setting of circuits to a defined state so that a test process can proceed in a predefined manner.
Intermittent Fault	A fault that appears and disappears over time.
Life Cycle Cost	Costs incurred during the life of a design (development, manufacture, installation, operation and maintenance).
Level Sensitive Scan Device	A structures scan technique.
Maintainability	Ease with which a system fault can be detected, isolated, and repaired.
MIL-STD-2165	Testability Program for Electronic Systems and Equipment
Node	An electrical connection between two or more components.

Observability	The degree to which a signal can be monitored.
Off-line BIT	BIT that runs periodically in the background of functioning equipment.
On-line BIT	BIT that runs once at power-up and whenever commanded by a controller.
Parity Code	A method of adding an extra bit(s) to data or data transmission which when added to the data bits will sum to an odd or even number. An error exists if the sum is not the in the expected state - odd or even.
Partitioning	Physical or logic division of circuitry into smaller more testable sections.
Pave Pace	1990s USAF program with advanced reliability objectives of yielding a 500 hour MTBF of LRUs.
Pave Pillar	1980s USAF program with reliability objectives of yielding a 70 hour MTBF of LRUs.
Prognostics	Predicting faults.
Race Condition	The timing fault that happens when a signal violates set-up times and circuit delays. This leads to unpredictable outputs.
Random Access Scan	A scan technique.
Reliability	The conditional probability that the equipment will operate properly after working correctly at t = 0.
Residue Code	Error-detecting/correcting arithmetic codes used during arithmetic operations.
Scan Path	A testability technique which replaces normal latches in a device which latches which can be configured as shift registers (SRLs).
Scan/Set Logic	A scan technique.
Sequential Circuit	A circuit which has an output that is dependent on the present inputs of the circuits and one or several previous inputs. All circuits with registers are sequential circuits.
Smart BIT	A BIT technique which incorporates environmental and stress parameters with performance to determine if a fault ocurred due to an over-stress condition in fault-free equipment.

Synchronous Several signals are synchronous if one is an integer multiple of the other and they are in phase.

Testability An aspect of a design that influences ease of developing tests, thoroughness of tests (FAR, accuracy), and limiting costs and time (MTTR, MTBF) incurred by test development, test, and test support.

Transputer A microcontroller used specifically for parallel processing.

Triple Modular Redundancy A fault masking technique which uses three redundant circuits with outputs that are input to a voting circuit.

Weighted Random Process Pseudo-random patterns with weighted ratio of ones to zeros.

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